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Fabrication of vertical nanopillar devices

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Abstract

Electron transport in silicon nanopillars has been investigated, with a view to developing vertical electron emission, electroluminescent and photoluminescent devices. Arrays of nanopillars were fabricated in highly-doped single crystal silicon and polysilcon materials. A 'natural lithography' technique utilising colloidal gold particles as an etch mask, in conjunction with standard microfabriction techniques, was used to fabricate the nanopillars in selected regions. The pillar height was 100 nm in single crystal silicon material and 40 nm in polysilicon material and the diameter of the pillars was 30 nm. A top contact was supported on a polyimide film, deposited by spin coating and curing, and then etching-back in oxygen plasma to expose the pillar tops. The current–voltage characteristics of these devices were measured at range of temperatures.
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1. Introduction

Vertical nanopillar devices in silicon and polycrystalline silicon are of great interest for the investigation of electron emission, electroluminescence (EL) and photoluminescence (PL) [1–3]. The nanometer-scale size of nanopillars leads to electrical and optical properties different from those of bulk silicon. While bulk crystalline silicon is an indirect band gap material, visible photoluminescence has been observed from nanometre sized silicon structures [4]. Attempts have been made to investigate the EL and PL from nanopillar arrays, e.g. EL devices reported by Nassiopoulos et al. used nanopillars defined by deep UV lithography and reactive ion etching [1]. However, the device operation and electron transport are not fully understood. It was suggested that an investigation of the EL dependence on electrical current, voltage, and temperature could clarify the device operation. It was also pointed out that the device efficiency could be improved by increasing the pillar density. Malinin et al. fabricated EL devices where pillars were fabricated using a self-organised gold–chromium mask and reactive ion etching [2]. In these devices there was variation in pillar diameter and shapes.

The fabrication of nanopillars for these devices can be achieved by a large number of techniques, such as electron-beam lithography [5], the use of scanning tunnelling microscopes [6], 'scratch' lithography [7], cluster-beam deposition of metallic etch masks [8], laser irradiation [9], and colloidal gold natural lithography [10]. Each of these techniques has limitations. For example, while nanopillars defined by electron-beam lithography exhibit high uniformity and high resolution [5], low throughput limits the number of pillars fabricated. This makes electron-beam lithography unsuitable for experiments and applications

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requiring both high uniformity and high density of nanopillars. The ultimate objective for nanopillar fabrication is a high throughput technique yielding uniform ~10 nm diameter nanopillars of high aspect ratio, with uniform coverage of the entire sample. Colloidal gold lithography techniques meet all four requirements of uniformity, small dimensions and high aspect ratio [10].

In this paper, we present a technique for the fabrication of vertical nanopillar devices using colloidal gold lithography in conjunction with standard microfabrication techniques. In this technique, there is no variation in pillar diameters and shapes in contrast to previously reported nanopillar devices [1,2]. Furthermore, the nanopillar density can be increased by increasing the colloidal particle deposition time. Therefore, the device efficiency can be increased [1]. We also measured the current–voltage characteristics of the fabricated devices from 300 to 25 K, in order to test the device design. With a reduction in the top contact to ~15 nm, these devices may be used to investigate electron emission, EL and PL from nanopillar arrays [1,2,11].

2. Fabrication process

A schematic diagram of the device is shown in Fig. 1. The devices were fabricated in SOI wafers with a ~200 nm top silicon layer. The layer was n-doped to a concentration of $1 \times 10^{19}/\mathrm{cm}^3$. The processing steps are now discussed in detail.

2.1. Nanopillar fabrication

The nanopillars were fabricated using colloidal gold particle lithography, in combination with electron-beam lithography. Firstly, the regions where the pillars were to be fabricated were defined by e-beam lithography. The native silicon dioxide layer was stripped-off from these regions using a SILOX etch for 30 s.

The nanopillars were then fabricated by a lithography technique utilising a gold colloidal particle monolayer as an etch mask, using the process developed by Lewis et al. [10]. After the SILOX etch, the samples were baked at 120 °C. The samples were then immersed for 5 min in a solution of ‘APTS’ [3-(2-aminoethylamino) propyltrimethoxysilane], which acts as an adhesion agent between the colloidal gold particles and the silicon layer. The chip was then baked at 120 °C and immersed in a solution containing a suspension of gold particles. The samples were inspected using a Hitachi S-900 scanning electron microscope to check the quality of the deposition. Fig. 2a shows a micrograph of the sample with 30 nm colloids. The samples were then etched anisotropically for 45 s using reactive-ion etching (20 sccm $SiCl_4$ and 20 sccm CF_4 at 20 mTorr, 0.42 W/cm^2). The resulting pillars were 30 nm in diameter and 100 nm in height. Fig. 2b shows the edge of region where the pillars were fabricated. Fig. 2c shows a high-resolution scanning electron micrograph of the nanopillars.

Here, the discussion is confined to devices with 30 nm diameters. However, devices with different pillar diameters were also fabricated using colloidal particles of different diameters. Devices with pillar diameters 5 nm, 10 nm, 15 nm, 20 nm, and 60 nm were obtained as well. For smaller diameter nanopillars, the maximum pillar height obtained was relatively smaller as compared the larger diameter nanopillars. In these devices, the pillar height was also varied, depending upon the reactive ion etching time. Furthermore, the pillar density could also be varied by varying the colloidal particle deposition time.

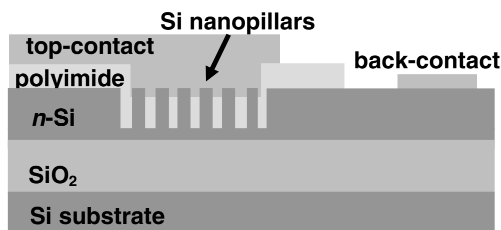

Fig. 1. Schematic diagram of a Si nanopillar device.

2.2. Surface planarisation and electrical isolation of pillars

The electrical isolation of the pillars and surface planarisation was achieved by spin coating and curing a polyimide film, and then etching-back in oxygen plasma to expose the pillar tops. The polyimide material was supplied as a polyamic acid (know as the polyimide precursor) that could be applied by spin coating. It was then cured by heating, during which the polyimide was chemically altered to form a solid, highly stable layer. A polyimide PI 2555 from DuPont’s pyralin range [12] was used. This was found to

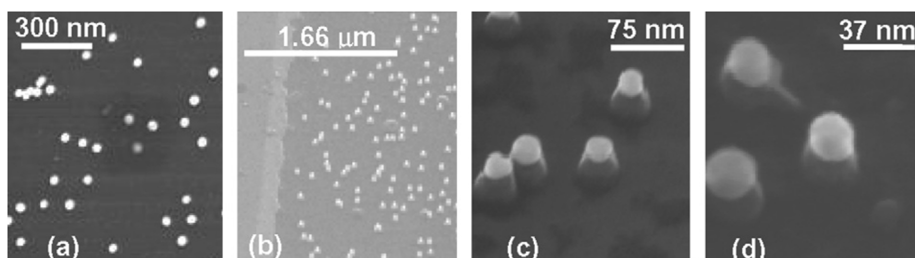

Fig. 2. Scanning electron micrograph of: (a) 30 nm gold colloidal particles deposited on n-Si, (b) edge of a region with nanopillars, (c) nanopillars after reactive ion etching with colloidal particles on top and (d) nanopillars coming out of polyamide film after etching in oxygen plasma.

have the required film thickness, planarisation, adhesion and shrinkage properties for our application. The polyimide precursor was spun onto the sample at 8000 rpm for 120 s. Nitrogen gas was then blown onto the sample after 20 s, and this was found to reduce edge build-up effects [13]. The spin speed and time were the maximum available in our spinner and resulted in a film thickness ∼1 μm thick.

The film was then soft baked at 120 °C for 30 min to remove any solvents in the film. The film was then 'imidised' i.e. cured in an oven. Here, the oven was ramped up to ∼252 °C over 90 min and then held at the maximum available temperature for an additional 60 min. The temperature cycle imidised the film to well over 90%. This temperature cycle was acceptable as long as the maximum baking temperature was not exceeded in subsequent fabrication steps.

2.3. Masked etch back

Oxygen plasma was used to etch the polyimide to expose the top of the pillars for the top contact, and to the substrate to make the back contact. Two layers of A8 PMMA resist were spun and cured at 180 °C for 1 h to give a layer about 1.5 μm thick. This layer was then patterned using e-beam lithography and developed. The polyimide was then etched back in a Plasmaprep 300 oxygen plasma barrel etcher. The chamber pressure used was 0.3 Torr and the etch power was 400 W. The etch rate for the polyimide was 5 nm per minute and the etch rate for PMMA was approximately 25 nm per minute. The chips were then etched for 100 min.

After removal of the remaining A8 in acetone and IPA, two fresh layers of A8 resist were spun-on and cured as before. The pattern used this time allowed etch-back to expose the pillar tops. This could be completed without excessive thinning of the polyimide in other areas still covered by resist.

After development, the devices typically required another 2–3 h of etching in the oxygen plasma. The approximate film thickness could be determined by using the colour of the film under white light to estimate the film thickness. When the pillar tops were almost exposed, frequent SEM examination was required to control the etch-back accurately until the pillar tops only were free of the polyamide. A scanning electron micrograph of a pillar after etch back is shown in Fig. 2d.

2.4. Fabrication of contact pads

The final fabrication stage defined electrical contacts to the top of the pillars, and to the substrate. Electron-beam lithography was used to define the 300 nm thick Au upper contact, using evaporation of the Au followed by and lift-off in acetone. Finally, the substrate contact was patterned using electron-beam lithography, and the evaporation of 30 nm chromium and 300 nm gold. Lift-off in acetone completed this process.

3. Results and discussion

The electrical measurements presented here are from devices measured using a cryogenic temperature prober BCT-43MDC from Nagase & Co. Ltd. with a base temperature of about 20 K, and an Agilent 4156A parameter analyser.

Fig. 3a shows the current–voltage (*I–V*) characteristics of a vertical nanopillar device of area ∼16 μm^2. The device consisted of a nanopillar array with 30 nm diameters and 100 nm high pillars. Within this device, ∼600 of nanopillars were present, estimated from the packing density. The pillars were in contact with the silicon below and with the top-metal contact above. The polyimide planarised layer containing the pillars acted as an insulator, in which the pillars were embedded. The *I–V* characteristics show only a small current ∼1 nA at low bias less than ∼|1.5| volts. This suggests that a potential barrier to conduction exists in the pillars. Because of the surface depletion effects in the nanopillars, the pillars are likely to be fully depleted, forming an i–n diode at the pillar–substrate interface. The Au–

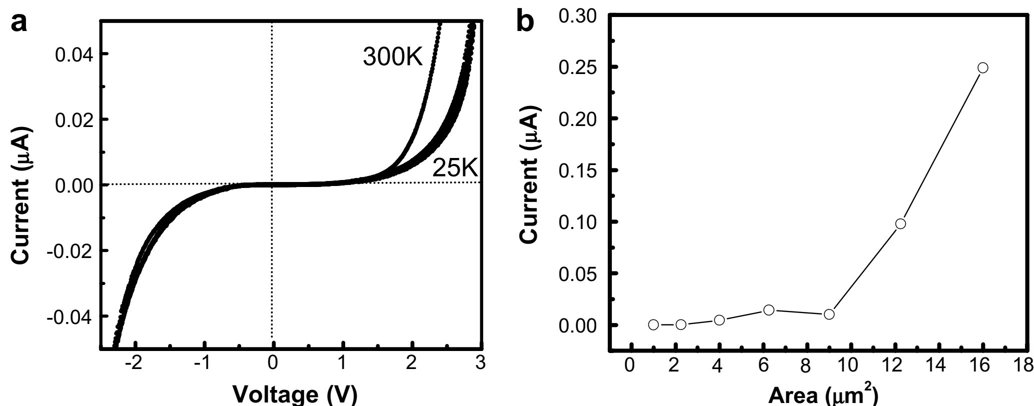

Fig. 3. (a) *I-V* characteristics of a vertical nanopillar device with an area of 16 μm^2 from 25 to 300 K in steps of 25 K and (b) current vs. area plot for vertoical nanopillar device at 3 V.

pillar interface can also form a Schottky junction. Under the positively biased conditions (positive bias applied to the top Au contact) above a turn-on voltage of ~1.5 V, electrons are thermally injected from the n-type substrate into the wires drift towards the metal electrode. A similar kind of operation mechanism has been suggested for electroluminescent devices based on silicon nanopillars [1,2] and ballistic electron emitting porous silicon diode [14].

Fig. 3b shows the scaling of the current in these devices with area at 3 V. The figure shows that there is considerable increase in the current for large area devices from 12.25 μm^2 to 16.0 μm^2. There is however only small increase in the smaller devices from 1.0 μm^2 to 9.0 μm^2. This may be associated with the polyimide etching processes. We have noted that the polyamide etching was better for large area devices as compared to those with smaller area.

4. Conclusions

Vertical nanopillar devices were fabricated in n-Si and polysilicon materials using colloidal gold lithography in conjunction with electron-beam lithography, reactive ion etching and metallisation. Devices of different areas ranging from 1 μm^2 to 16 μm^2 were fabricated. In these devices, nanopillars of different diameters and heights were used. The gaps between the pillars were filled by spin coating and curing a polyimide film. The pillar tops were then exposed to deposit the top contact, by etching the excessive polyimide in oxygen plasma for ~300 min. To make the contact to the bottom of the pillars, the polyimide was further etched for 100 min from a selected region. The electrical contacts were then deposited by evaporating 300 nm gold in vacuum. The *I–V* curves of these devices were measured at temperatures ranging from 300 to 25 K. By reducing the thickness of the top contact to ~15 nm these devices may be used as electron emission, electroluminescent and photoluminescent devices.

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