Nanosilicon single-electron transistors and memory

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Abstract

Nanosilicon materials are promising systems for the fabrication of single-electron transistor and memory devices in silicon. In these devices, precise control over the charging of a nanometre-size 'island' by just one electron raises the possibility of low power, highly scaled integrated circuits with one electron per bit. Nanosilicon materials, consisting of crystalline silicon grains ~10 nm in size, provide a means to fabricate ultra-small charging islands using growth techniques rather than high-resolution lithography. It is then possible to fabricate single-electron devices operating at room temperature. This review introduces electron transport in nanosilicon and considers the design and fabrication of single-electron transistors, quantum-dot transistors, and few-electron memory cells in these materials.

1. Introduction

Nanoscale silicon materials [1-12], consisting of crystalline silicon grains ~10 nm in size separated by amorphous silicon or silicon oxide grain boundaries (GBs), have raised the possibility of the fabrication of advanced single-electron devices and circuits in silicon. In these devices, the single-electron charging or 'Coulomb blockade' effect [13-17] is used to control precisely the transfer of individual electrons on to a nano-scale conducting island, isolated by tunnel barriers. Single-electron devices are promising candidates for advanced logic and memory circuits where the bits can be defined using only a few electrons, leading to circuits with immunity from statistical fluctuation in the number of electrons per bit and very low power consumption. In addition, the inherently small size of these devices, and the potential for high scalability in comparison with conventional complementary metal-oxide-semiconductor (CMOS) devices, raises the possibility of very low power, highly integrated large-scale integrated (LSI) circuits.

The continuous reduction in size of microelectronic devices has been the key to rapid improvement in the performance of CMOS LSI circuits. In 2004, the MOS transistor minimum feature size (transistor gate length) was ~45 nm [18]. It is predicted that by 2010, this will fall to 18 nm and that it may be possible to accommodate ~1 billion transistors on a microprocessor chip. With each design generation, it has been possible to incorporate ever greater numbers of transistors and memory cells on to a single memory or logic chip, accompanied by a rapid increase in the operating speed of the chip. However, increasing the speed and number of transistors on the chip has lead to a sharp rise in the total power consumption of the chip. For example, in microprocessors, although the power consumption of the industry-standard metal-oxide-semiconductor (MOS) transistor has been reduced by a factor of ~2 every five years, due to a reduction in size and improved operating parameters, the rise in the number of transistors per chip has more than negated this improvement. The result has been a ~3.5 fold increase in the total power consumption of the microprocessor during the same period.

A reduction in the number of electrons necessary to define the storage 'bits' would automatically lead to smaller operating currents and lower power consumption. Unfortunately, a reduction in the number of electrons per bit in a conventional MOS transistor to well below ~100 is difficult because '$\sqrt{n}$' fluctuations in the electron number cause unacceptable statistical fluctuations in the sub-threshold characteristics of the MOS transistors [19]. In addition, if the size of the device falls to below ~10 nm, then quantum effects can influence strongly the device characteristics. Perhaps the most significant of these effects for conventional MOS devices is the quantum tunnelling of electrons across thin potential barriers. This can lead to increasing gate leakage currents in MOS transistors, with an accompanying loss of gain and an increase in the power consumption.

An additional problem, especially significant for memory circuits, arises in both storing and sensing small numbers of electrons per bit, well below ~1000. If we consider scaling trends in dynamic random access memories (DRAMs) [20], after the 1 Mbit generation, it has become increasingly difficult to maintain a continuous decrease in the charge per bit. This is because the signal associated with this charge becomes difficult to sense, and is less immune to leakage current, internal noise and

soft errors. There has been a strong effort to scale down the cell area while maintaining the number of stored electrons at ~50,000. As a result, the design of the standard 1-transistor, 1-capacitor, DRAM cell has become increasingly complex. In this regard, a 'gain-cell' approach, where a transistor integrated in each cell amplifies the stored charge directly (e.g. a high-speed analogue of a 'FLASH' type memory cell), may be promising [21, 22].

Silicon single-electron devices can help in overcoming the power consumption, charge fluctuation and charge sensing problems in LSI circuits scaled into the ~10 nm size regime. In these devices, the precise definition of bits by a few or even single electrons using the Coulomb blockade effect directly leads to immunity from charge fluctuations and low power consumption. The performance of single-electron devices can also improve with a reduction in device size. The devices also retain compatibility with LSI fabrication techniques, which would allow integration with CMOS technology for those sections of the circuit where conventional MOS devices would still be appropriate [4]. In would then be possible to fabricate highly scalable, inherently low power, few-electron LSI circuits.

Nanosilicon materials provide a highly promising approach for the fabrication of CMOS compatible single-electron devices and circuits. Using nano-scale silicon grains and the surrounding GBs to define the critical components of the device, i.e. the charging 'island' and the surrounding tunnel barrier, can allow the 'natural' fabrication of devices using growth techniques rather than high-resolution lithography. We note that if the grains are ~10 nm or less in size, and the GB tunnel barriers are ~100 meV or higher, then the single-electron charging energy and tunnel resistances can be large enough for room temperature operation of the nanosilicon single-electron transistors [5, 13, 23]. In devices of this scale, quantum confinement of electrons is also likely, raising the possibility of quantum dot devices [24, 25] in silicon. This may be more easily realisable using nanosilicon material rather than using high-resolution lithography. It is also possible to control the size and shape of the nanosilicon grains in these materials, with precision greater than is possible with high-resolution lithographic techniques, by carefully tailoring the material growth process [7, 8, 10, 11]. This would help to obtain reproducibility between the operating characteristics of the large numbers of devices necessary in LSI circuit applications.

In this review, we will introduce briefly single-electron charging, Coulomb blockade, and quantum effects with reference to nanosilicon. We will then consider the design and operation of single-electron and quantum-dot nanosilicon transistors, Finally we review work on nanosilicon memory devices, where silicon nanocrystals can be used to store charge consisting of only a few or even single electrons.

1.1. Single-electron and quantum confinement effects

We now introduce briefly single-electron charging effects in silicon. Detailed general introductions to single-electron charging effects can be found in Ref. [13-16]. Consider a system where electrons tunnel across a small conducting 'island', isolated between source and drain electrodes by tunnelling potential barriers (Fig. 1(a)). We assume that the tunnel barrier resistances R_1 and R_2 (circuit diagram, Fig. 1(b)) are large enough such that the electronic states on the island are relatively localised. This condition exists if R_1 and R_2 are greater than the quantum of resistance $R_K \sim h/e^2 =$

26 kΩ. If the capacitances associated with the tunnel barriers are C_1 and C_2, and the total capacitance of the island $C_1 + C_2 = C \sim 10^{-15}$ F or less, then the charging energy $E_c = e^2/2C$ associated with the addition of even a single electron on to the island may be larger than the thermal energy $k_B T$ at low temperature. This implies that electronic conduction can begin across the system at low temperature only if the applied voltage across the drain and source electrodes V_{ds} is larger than $2E_c/e$ (assuming that an equal voltage drop occurs across each tunnel junction) This is the well-known 'Coulomb blockade' of conduction, leading to a low current voltage gap in the *I-V* characteristics.

Once the Coulomb blockade is overcome, electrons can transfer on to and off the island, a drain-source current I_{ds} begins to flow, and the average number of electrons on the island increases by one. As the applied voltage equals multiples of $2E_c/e$, the charging energy for additional electrons on the island is overcome, and the average number of electrons on the island can increase one-by-one. There is a set of discrete energy levels on the island, separated by the single-electron charging energy $e^2/2C$ (Fig. 2(a)) If the source-island and drain-island tunnel resistance are similar, then electrons can tunnel off the island at the same rate as they tunnel on to the island, and the current increases linearly with voltage outside a central Coulomb blockade region $V_{cg} = 2e/C$ (dashed lines, Fig. 2(b)). However, if the tunnel resistances are very different then electrons can persist on the island, influencing the tunnelling probability of additional electrons and leading to current steps periodic in voltage. This is called the Coulomb staircase (dotted lines, Fig. 2(b)), and each step corresponds to the addition of an extra electron on to the island. We note that the drain-source conductance shows a peak at each current step in the staircase.

It is also possible to use an additional gate electrode to control the island charging (Fig. 3(a)). If the gate voltage V_{gs} is varied, the charging energy is periodically overcome and drain-source current or conductance oscillations periodic in gate voltage are observed (Fig. 3(b)). Each oscillation corresponds to resonance of the single electron levels with the Fermi energy of the drain. Passing through an oscillation changes the number of electrons on the island by one, e.g. if the gate voltage becomes more positive at an oscillation, the single-electron level energy is lowered relative to the drain Fermi energy, and an electron can occupy the level. The oscillation period is given by $\Delta V_g = e/C_g$. Such a device is known as a single-electron transistor (SET), demonstrated first by Fulton and Dolan [26] in 1987, used an $Al/Al_2O_3/Al$ multilayer structure operating at 4.2 K. Here, both the drain-source voltage and the gate voltage can control the number of electrons on the island.

Figure 4 shows schematically the 'charge stability diagram' of a SET, where the electron number on the island of the SET is plotted as a function of the drain-source voltage and the gate voltage. It is seen that this number is constant within trapezoidal regions of charge stability, often referred to as 'Coulomb diamonds'. The edges of the charge stability regions trace the position of the single-electron conductance oscillation peaks, as a function of the gate and drain-source voltage. The electron number is seen to change by one from a charge stability region to the next.

We note that the single-island SET can be very sensitive to changes in the charge on the gate capacitor, or simply the background charge (often called the 'offset' charge) nearby the island. A change in this charge of *e/2* can shift the SET operating

point from the middle of the Coulomb gap to the edge of the Coulomb gap. This sensitivity can be a potential problem for single-electron circuits, leading to unwanted switching of the SET, but can be overcome by using silicon SETs, where most traps serving as the source of offset charge may be passivated using oxidation. In addition, a multiple tunnel junction (MTJ) SET may be used, where there are a number of charging islands in series. Any fluctuation in a local 'offset' charge then switches only one of the islands of the SET, but not the others, reducing sensitivity of the entire device to the 'offset' charge.

Single-electron charging effects were first observed in a silicon system in 1989, when Scott-Thomas *et al* [27] observed conductance oscillations at 2 K in the inversion layer of a narrow channel MOSFET as a function of the gate voltage. This behaviour was explained by single-electron charging effects in a segment of the inversion layer, isolated by potential barriers associated with scattering centres [28]. Single-electron charging effects were then observed in other silicon-based systems, e.g. Coulomb blockade characteristics persisting up to 50 K were observed in a device with a nanometre-scale island fabricated in δ-doped silicon germanium [29], and in a nanometre-scale island defined using high-resolution electron beam lithography in the heavily-doped crystalline silicon top layer of silicon-on-insulator (SOI) material [30]. These observations opened the way for the development of silicon SETs compatible with CMOS technology.

If the island in a SET in SOI is scaled down to very small island sizes ~12 nm, then single-electron conductance oscillations can be observed even at room temperature [31]. It is also possible to obtain room temperature SETs using ~10 nm size nano-scale islands isolated by pattern-dependent oxidation. [32]. Single-electron effects can also occur in conduction through etched nanowires defined in SOI where there is no lithographically defined island. Ishikuro *et al* [33] have observed single-electron effects at room temperature in ~10 nm wide and 100 nm long anistropic wet-etched nanowires. It is believed that in a manner similar to single-electron effects in narrow inversion layers in Si MOSFETs, potential fluctuations isolate segments along the nanowire, creating an MTJ device. These fluctuations have been associated with disorder in the local doping level or surface potential [34], and with lateral confinement effects or regions of SiO_x [35]. Heavily doped gated nanowires have been modelled as an MTJ with a combination of single-electron effects and a field effect induced by the gate voltage [36]. These devices are easier to fabricate because precise, high-resolution lithography to define the charging island is unnecessary. However, the random nature of the MTJ leads to more complicated electrical characteristics.

In nanosilicon films, the grains can be < 10 nm in size and the grain capacitance can be extremely small, ~1 aF. We may estimate the order-of-magnitude of the charging energy for a nanoscale dot of radius r = 5 nm embedded in SiO_2, using the self-capacitance of a sphere $C = 2\pi\varepsilon r$ = 1 aF. This implies that the single-electron charging energy, $E_C = e^2/2C$ = 74 meV, which is greater than k_BT = 25 meV at room temperature (T = 300 K). This implies that single-electron charging effects may be observed even at room temperature in these materials [5, 23].

In nanosilicon films with grains ~10 nm or less in size, an additional effect is the quantum confinement [24, 25] of electrons on the grain by the GB potential barriers,

leading to the formation of discrete electron energy levels. For example, if we consider a grain of width 'r' with vertical potential barriers, the electrons then occupy discrete energy levels within the well, where the energy level spacing $\Delta E \sim \pi^2 \hbar^2/2mr^2$. Such a system forms a 'quantum dot', leading to strong peaks in the electron tunnelling probability across the grain when the levels align with the Fermi energy. Placing the quantum dot between source and drain contacts provides a means to observe resonant tunnelling through these levels. Strong tunnelling peaks are observed when the energy levels in the dot align with the Fermi level in the source as a function of the source-drain or gate bias. We note that usually, a combination of single-electron and quantum confinement effects can occur. Here, the energy of each level is given by the sum of the quantum confinement and single-electron charging energies.

2. Nanosilicon single-electron transistors

2.1. Conduction in continuous nanocrystalline silicon films

We will consider first the electronic conduction mechanism in a doped, physically continuous polycrystalline or nanocrystalline silicon (nc-Si) thin film, before extending this picture to include single-electron and quantum confinement effects associated with nanoscale grain sizes. Conduction through a nc-Si film is strongly affected by potential barriers at the GBs, associated with the large density of trapping states caused by defects at the GBs. These states trap free carriers from the grains, reducing the carrier density within the grain. The space charge distribution near the GB also leads to an electric field, which causes a 'Schottky-like' potential barrier at the GBs [37-40]. The height and width of the potential barrier is a function of the doping concentration in the grains. The carrier density in the grains may also be reduced if any segregation of dopant atoms occurs at the GBs [39, 41, 42].

Consider a one-dimensional chain of n-type nanocrystalline silicon grains (Fig. 5(a)), where the GB thickness is small relative to the grain size 'D'. We assume a uniform donor concentration N_D (per unit volume) in the grain, and GB traps with a density N_t (per unit area) at an energy E_t w.r.t. the intrinsic Fermi level. We note that in large grained polycrystalline silicon films, N_t is often $\sim 10^{11} - 10^{12}$ /cm^2 [40, 43]. Charge trapped at the GBs leaves ionised donors in the grains (Fig. 5(b)). For small N_D, all the electrons contributed by the dopants are trapped in the GBs and the grain is fully depleted. The trapped charge and the ionised dopants generate an electric field extending from the GB into the grains, leading to a double Schottky-like potential barrier of height E_{GB} (Fig. 5(c)). As N_D increases, more charge is trapped at the GB, increasing the electric field and potential barrier height until at $N_D = N_D^* \approx N_t / D$, the conduction band in the centre of the grain lies near the Fermi energy E_F. Free carriers can now exist in the grain and E_{GB} is at its maximum value. Any further increase in N_D reduces E_{GB}. In the above discussion, we have assumed that N_t is high enough such that all the traps are not filled if N_D is increased. In addition, in a real nc-Si film, the grain size, GB trap density, and local doping concentration is likely to vary from grain to grain, leading to a distribution of GB barrier heights and widths across the film [44].

Electron transport across the GBs at room temperature, and at moderately low temperature, can occur by thermionic emission. With this mechanism, the temperature

dependence of the conductance, plotted as an Arrenhius plot, ln(G) v.s. 1/T, will be linear. However, the conduction mechanism may be assisted by tunnelling via defect states within the barrier, e.g. by empty states at the GB, or by tunnelling across the entire barrier if the barrier width is small. As the temperature is reduced, the thermionic emission current falls and tunnelling effects begin to dominate the conduction process, leading to a largely temperature-independent section of the Arrenhius plot. This is shown schematically in Fig. 6. The slope of the temperature dependent section of the plot can be used to extract the activation energy, which is a measure of the barrier height. At low temperatures, a variable range hopping transport mechanism may also contribute to the overall conduction in a nanocrystal solid [45, 46]. In addition, any variation in the barrier heights and widths across the film can result in a network of percolation paths for current flow across the film [44, 45], where low resistance paths through GBs with low potential barriers dominate the conduction.

In the preceding discussion, we have ignored single-electron charging effects in the silicon grains. A thermionic emission model is valid if the grain size in the nc-Si is large enough, or the temperature is high enough such that the thermal fluctuations k_BT are greater than the single-electron charging energy $E_c = e^2/2C$. The thermionic emission model will also be valid if the GB barrier height and width is small enough that the associated tunnel resistance R_{GB} is comparable to or smaller than the quantum resistance $R_Q = h/e^2 \sim 22.5$ kΩ, i.e. electrons can be delocalised across the grains.

We will now consider the influence of reducing the grain size in a polycrystalline silicon film to the nanometre-scale. Typically, 'quantum effect' nc-Si devices have grain sizes from ~50 nm to less than 10 nm. As the grain size is reduced to the nanometre scale, the local or 'microscopic' properties of the GBs, single-electron charging effects and quantum-confinement effects all begin to affect the electron transport mechanism [13, 25, 47, 48]. We have seen that the nc-Si film may be regarded as an array of nano-scale conducting grains, isolated from each other by potential barriers at the GBs. We have also seen that at cryogenic temperatures, electron transport can occur by tunnelling through the GB potential barriers. The nc-Si film under these conditions can then be considered to form a nano-scale tunnel capacitor network, which can show single-electron charging effects. If the grains are ~10 nm in size, then it is possible for the capacitance C to be as low as 10^{-18} F. The charging energy E_C can then be larger than $k_BT \sim 25$ meV even at room temperature. However, for the observation of room temperature single-electron charging, it is also necessary for the GB barrier height to be considerably larger than the thermal energy k_BT, and the GB tunnelling resistance $R_{GB} > R_Q$, so that electrons can be quasi-localised on the grains at room temperature. Coulomb blockade then occurs in the I_{ds}-V_{ds} characteristics across the grain, and current can flow only if $|V_{ds}| > |V_C|$, corresponding to the voltage necessary to overcome E_C. In addition, with grains ~10 nm or less in size, quantum confinement of electrons on the grains by the GB potential barriers is also possible, leading to the formation of discrete electron energy levels. A parabolic potential well picture may be expected from a simple extension of the polycrystalline silicon model discussed earlier. The electrons then occupy equally spaced energy levels within these wells and the grains form silicon 'quantum dots'. The *I-V* characteristics through these systems can then show current peaks associated with resonant tunnelling through the energy levels.

It is clear that single-electron and quantum-confinement effects may be of considerable importance in individual grains in an nc-Si film. However, in a large area film, variation in the grain size and in the tunnel barriers at the GB leads to percolation through the lowest resistance transport paths [47, 48]. This would tend to bypass the higher resistance paths associated with the grains behaving as quantum dots, and prevent the observation of single-electron and quantum confinement effects. Therefore, it has been necessary in most demonstrations of single-electron charging and quantum dot devices to reduce the number of current paths by defining nanowires and 'point-contacts' (i.e. a short nanowire where the length ≈ width). Depending on the geometry, one or multiple grains can contribute to single-electron charging effects, leading to single-island or MTJ devices.

2.2. Silicon nanowire single-electron transistors

The silicon nanowire SET in a continuous nc-Si film is an analogue of the widely investigated silicon nanowire SET fabricated in crystalline silicon-on-insulator (SOI) material (Sec. 1.1 and Refs. [30-35]). Crystalline silicon nanowire SETs mostly use a nanowire < 50 nm wide, defined by trench-isolation between large source and drain regions in the top silicon layer of the SOI material, ~50 nm or less in thickness and heavily-doped *n*-type (~ 10^{18} / cm^3 – 10^{20} / cm^3) or *p*-type (~10^{20} / cm^3). Disorder associated with the doping and with surface states results in a chain of conducting silicon islands along the nanowire, separated by depleted silicon potential barriers. At low temperature, the nanowire forms a MTJ system where conduction across the potential barriers occurs via single-electron tunnelling [34]. The position of the depleted silicon potential barriers can be controlled by patterning notches in the nanowire [30], or by forming potential barriers associated with self-limiting oxidation at the ends of the nanowire [32]. The nanowire current can be gated using a variety of techniques, e.g. trench isolated side-gates [34], deposited polycrystalline silicon or metal top gates [33], or a back gate formed by the substrate of the SOI material [30].

Nanocrystalline silicon nanowire SETs, very similar in geometry to these crystalline silicon SETs, can be defined in polycrystalline or nc-Si films less than ~50 nm thick. The different variations of gate structures for SOI nanowires can also be applied here. However, the presence of GBs creates tunnel barriers intrinsically along the nanowire, isolating charging islands at the grains, and any doping or surface disorder effects are likely to be subsidiary to this. Disorder can however affect the GB potential barrier shape, by altering the local space charge distribution.

Lateral, side-gated nanowire SETs have been fabricated in solid-phase crystallised (SPC) polycrystalline silicon films, deposited on SiO_2 layers grown on silicon substrates [49, 50]. Figure 7(a) shows a schematic of a typical device. The polycrystalline silicon material was prepared using a standard LSI process, as follows: A 50 nm thick amorphous silicon film was first deposited at 550°C by plasma enhanced chemical vapour deposition (PECVD), onto a 10 nm or 40 nm thick gate quality silicon oxide layer grown on a crystalline silicon substrate (*p*-doped, at 5 3 10^{14} cm^{-3}). Phosphorous ion-implantation was used to heavily-dope the film *n*-type to 5 3 10^{19} cm^{-3}. The film was then crystallized into polycrystalline silicon using thermal annealing at 850°C for 30 minutes. TEM analysis indicated that the grains varied from ~5 nm – 50 nm in size, and the average grain size was ~20 nm. Side-gated nanowires of various geometry were defined in the film using electron-beam

lithography and reactive-ion-etching in a $SiCl_4$ / CF_4 plasma. Nanowires of various dimensions, and with argon annealing or oxidation treatments were fabricated. Figure 7(b) shows an SEM image of this type of device after oxidation, where the nanowire is 1 μm long and 40 nm wide. The oxidation process reduces the cross-sectional area of the nanowire by ~10 nm and passivates surface states. The annealing process modifies the defect state density at the GBs, at the Si/SiO_2 interface and along the etched surfaces, and increases the grain size.

The drain-source I_{ds}-V_{ds} characteristics at 4.2 K, from an oxidized nanowire where the pre-oxidized width was 50 nm and length was 1.5 μm, are shown in Fig. 8(a) [49]. The characteristics show single-electron charging effects associated with the charging of the crystalline silicon grains along the nanowire, isolated by tunnel barriers at the GBs [49, 50]. A zero current Coulomb gap, and the steps of a Coulomb staircase can be identified. Single-electron current oscillations are observed in the I_{ds}-V_{gs} characteristics (Fig. 8(b)), corresponding to the addition of single electrons on to a dominant charging island. The single-electron current oscillations in various devices can be complex, due to multiple periods associated with an MTJ and to changes in the gate capacitance with voltage. This device had a rather low maximum operating temperature of ~15 K, due to the large grain size and low GB tunnel barriers heights.

The single-electron characteristics of these devices are dependent on the nanowire dimensions [50]. The oscillation periods increase when the nanowire length is increased from 500 nm–1.5 μm, and decrease when the nanowire width is increased from 50 nm to 60 nm. Wider wires show only Ohmic conduction. This is because the longer the nanowire, the higher is the probability of smaller grains existing along the nanowire, with smaller gate capacitances and larger observed oscillation periods. The decrease in the oscillation period with increasing width, which implies an increase in the lateral area of the charging island, can be associated with the electric field through the buried oxide, below the plane of the side-gates and nanowire.

The effect of the grain size in nc-Si SETs can be observed directly in the single-electron characteristics, as this is proportional to the island capacitance and therefore determines the Coulomb gap and the current oscillation period. However, the GB tunnel barrier must be investigated by other means, e.g. by an Arrenhius plot measurement of the SET conductance as a function of temperature (Fig. 6). This allows an extraction of the thermal activation energy, which may be associated with the barrier height. This technique has been used to investigate the effect of restricting the multiple current paths in nc-Si nanowire SETs, by varying the dimensions of the nanowire. Furuta *et al* [47, 51] have investigated the electrical properties of a single GB at the microscopic scale using nanowires defined by electron-beam lithography in 50 nm thick polycrystalline silicon films with grain size from 20 nm – 150 nm, created by solid phase crystallisation of low-pressure chemical vapour deposition (LPCVD) deposited amorphous silicon. Furuta *et al* fabricated nanowires of varying width and length, from 30 nm – 50 nm, and measured the distribution of the potential barrier height from the Arrenhius plots. They observed that any local variation in the potential barrier height of a GB provided a low resistance path for current transport across the GB. If the nanowire width was increased, a lower barrier height was measured because of the increased likelihood of a low section of the GB across the nanowire. If the nanowire length was increased, a higher barrier height was observed

because more than one GB could lie in series, and the GB with the highest barrier was dominant.

We observe that the barrier height can vary even at various points along a single GB. This has strong implication for the fabrication of nanometre-scale electronic devices in nanocrystalline and polycrystalline silicon films. It is clear that disorder in the GB potential barrier can lead to considerable variation in the *I-V* characteristics of different devices, and that a means of control over the GBs may be essential for the practical fabrication of LSI circuits using nc-Si devices of small size. Careful optimisation of the polycrystalline silicon film growth or deposition processes may help to control the composition of the GBs.

2.3. Point-contact single-electron transistors: Room temperature operation

The maximum operating of nc-Si nanowire SETs may be raised up to room temperature if the grain size and the corresponding total grain capacitance is reduced. If the length and width of the device is also reduced to ~ 50 nm or less to form a 'point-contact' (Fig. 9(a)) then only a few grains can exist within the active area of the device at most, improving the electrical characteristics of the device. Such films have been deposited using VHF PECVD, where the film thickness was ~20 nm and the grain size was <10 nm [5], by using LPCVD where the film thickness was ~40 nm and the grains varied from ~10 – 30 nm in size [52], and by using extremely thin (<10 nm thick) granular and non-uniform films [5]. We will discuss SETs in granular films later (Sec. 2.5). In this section, we discuss the fabrication and characterisation of point-contact SETs in VHF PECVD nc-Si films, and the improvement of the operating temperature of these SETs to room temperature by selective oxidation of the GBs.

Point contact SETs which can operate up to 60 K have been fabricated in a ~30 nm-thick nc-Si, with grains <10 nm in size [53]. The films were deposited using VHF PECVD from a SiF_4 : H_2 : SiH_4 gas mixture, onto a 150 nm thick silicon oxide layer grown thermally on *n*-type crystalline silicon. The carrier concentration and electron mobility, measured at room temperature by Hall measurements, were 3×10^{20} /cm^3 and 1.8 cm^2/Vs respectively. Figure 9(b) shows a TEM image of the film, where uniformly distributed crystalline silicon grains can be seen (e.g. circled area). The grain size ranges from ~4–8 nm and the GBs were formed by amorphous silicon ~1 nm thick. The crystalline volume fraction, determined by Raman spectroscopy, was 70%. Point-contact SETs were defined in these films using electron-beam lithography in polymethyl methacrylate resist, and reactive-ion-etching in a mixture of $SiCl_4$ and CF_4 gases, in a manner similar to longer nanowire SETs. The point contact width was ~20 nm and two side gates could be used to control the device characteristics. Figure 9(c) shows a scanning electron micrograph of a device. These devices show Coulomb gaps ~40 mV which could persist up to a temperature of ~60 K. The single-electron current oscillations showed a main oscillation with a period of 500 mV in gate voltage. Finer superimposed oscillations were also observed, attributed to additional islands and the formation of an MTJ.

The operating temperature in these SETs is limited not only by the grain size and the associated inter-grain capacitances, but also by the tunnel resistance and height of the GB potential barriers. The low operating temperature of these SETs, even though

the grain size was small enough and the charging energy large enough to observe high temperature effects, could be associated with a comparatively low barrier height. The barrier height could be estimated using Arrenhius plots of the conductance of the device as a function of inverse-temperature (Fig. 10). Above a transition temperature $T_1 \sim 60$ K, the conduction mechanism could be attributed to thermionic emission across a distribution of potential barrier heights with various activation energies. The maximum gradient obtained in this region corresponded to an activation energy E_A ~40 meV, which could be associated with the maximum height of the amorphous silicon GB tunnel barriers. This is not high enough, relative to $k_BT \sim 25$ meV at room temperature, to confine electrons on the grains

The operating temperature of point-contact SETs in VHF PECVD nc-Si can be raised to room temperature by raising the GB tunnel barrier height, using selective oxidation of the amorphous silicon GBs into SiO_x [54-56]. These devices were again prepared in an *n*-type VHF PECVD nc-Si film with crystalline silicon grains 4-8 nm in size, and amorphous silicon GBs. However, the film thickness was only ~20 nm and in comparison with earlier work, the point-contact dimensions could be as small as 20 nm × 20 nm × 20 nm.

After defining the SET, a low-temperature oxidation and high-temperature annealing process was used to oxidise the GBs selectively. This process was performed after defining the SETs, in order to maximise the surface area for oxygen diffusion, and to passivate simultaneously the surface states in the device. A relatively low oxidation temperature of 750^{o}C for 1 hour was used, in order to take advantage of the higher rate of diffusion of oxygen atoms at these temperatures into the GBs than in the crystalline silicon grains. The devices were then annealed at 1000^{o}C for 15 minutes to improve the tunnel barrier height. Figure 11 shows an SEM image of a device. Microscopy of the SET before and after the thermal processing did not show significant change in the grain shape and size, due to encapsulation of the grains by SiO_x.

The selective oxidation of the GBs provides a method to engineer GB tunnel barriers with increased potential energy high enough to observe room temperature single-electron effects [54]. The source-drain current I_{ds}, measured with respect to the gate voltage V_{gs}, at temperatures from 23 K to 300 K, is shown in Fig. 12(a). Single-electron current oscillations with a single oscillation period of 3 V are seen, which can be associated with a single dominant charging island. The oscillations persist up to 300 K with an unchanged period. However, there is a fall in the peak-valley ratio as the temperature increases, due to a thermally activated increase in the tunnelling probability. Figure 12(b) shows the device I_{ds}-V_{ds} characteristics at 300 K, where a non-linearity corresponding to the Coulomb gap can be observed.

The room temperature operation of these devices can be attributed to the formation of SiO_x at the GBs, which leads to an increase in the tunnel barrier height and better confinement of electrons on the grains even at room temperature. The tunnel barrier height, measured using Arrenhius plots of the device conductance, is ~170 meV. This is approximately 7 times higher than k_BT at room temperature and considerably larger than the maximum barrier height of ~40 meV for a similar device in the as-deposited nc-Si film. The oxygen incorporation in the oxidised and annealed nc-Si film can be investigated using secondary-ion mass spectroscopy (SIMS) to

measure the oxygen depth profile [54]. It is seen that in a 30 nm wide point-contact, SiO_x with $x = 0.67$ was formed. Greater amounts of oxygen could be incorporated into the GBs in smaller point-contacts, due to diffusion from the sidewalls of the point contact. It is then possible for single-electron charging to occur on grains at the point-contact centre even at room temperature. This is shown schematically in Fig. 13.

In the preceding discussion, we have concentrated on single-electron effects only. However, in nc-Si SETs, quantum-confinement effects can also occur where the nc-Si grains not only exhibit single-electron charging phenomena but also show energy level quantisation. Such a combination of single-electron and quantum-confinement effects, along with resonant tunnelling through the discrete energy levels, is common in GaAs / AlGaAs two-dimensional electron gas devices at milli-Kelvin temperatures [13, 25]. The existence of discrete energy levels within silicon nanocrystals has been inferred from observations of light-emission from the nanocrystals [57-59]. In the electrical characteristics of a nanocrystalline silicon quantum dot transistor, these energy levels would lead to a complex series of resonant tunnelling peaks in the gate dependence of the transistor drain-source current. The peak separation corresponds to a sum of the single-electron and quantum-confinement energy level separation and the peak height corresponds to the coupling to the contacts of the electron wavefunction associated with each energy level. Natori *et al* [60] have theoretically investigated this behaviour for silicon dots. Interactions between two or more quantum dots are also possible, and both electrostatic and electron wavefunction coupling effects can be observed. We will discuss these effects in detail in Sec. 3.

Vertical transport polycrystalline and nanocrystalline silicon SET designs have also been demonstrated. Single-electron effects have been observed at 4.2 K in 45 nm – 100 nm diameter pillars formed in a material consisting of layers of polycrystalline silicon and Si_3N_4 [61]. In this device, the Si_3N_4 layers form the tunnel barriers and the polycrystalline silicon layers form the charging island. The lateral dimensions of the charging islands are defined not by the grain size but by the pillar sidewalls, i.e. lithographically. While the device does not show single-electron effects at room temperature, it can still be used as a vertical-transport switching device at room temperature. A vertical transport device has considerable advantages in device integration, e.g. it can be stacked on top of the gate of a MOSFET to form a random access memory gain-cell where the number of stored electrons can be as small as ~1000 [62]. This is a large reduction over the number of electrons used in a conventional one-transistor, one-capacitor DRAM cell and holds considerable promise for future advanced DRAM applications.

2.4. ‘Grain-boundary’ engineering

The previous sections have discussed the significance of the GB potential barrier in SETs in continuous nc-Si films. Control of the height of this barrier is crucial to the confinement of electrons on the grains at higher temperatures, and the operation of room temperature SETs. By contrast, the reduction of the GB potential barrier is important in reducing the film resistivity, and improving the effective carrier mobility in the nc-Si. Different ‘GB engineering’ processes can be used for these requirements.

The effect of oxidation and annealing on the electrical properties, and the structure of the GBs in heavily doped SPC polycrystalline silicon, has been

characterised in detail using bulk films, and using 30 nm-wide nanowires [63]. Oxidation at 650–750°C was seen to oxidise selectively the GBs, and subsequent annealing at 1000°C was seen to increase the associated potential barrier height and resistance. These observations were explained by structural changes in the Si–O network at the GBs, and the competition between surface oxygen diffusion and oxidation from the GBs in the crystalline grains. This work suggested that a combination of oxidation and annealing provided a method for better control of the GB potential barrier height and width in the polycrystalline silicon and nc-Si thin films.

In contrast, hot H_2O-vapor annealing effectively reduces the GB barrier height [64]. Experiments on nanowire devices fabricated in LPCVD polycrystalline silicon thin films showed that hot H_2O-vapor annealing effectively reduced the GB dangling bonds and the corresponding potential barrier height. In addition, the process narrowed the distribution of the barrier height value across different devices significantly. These effects could be attributed to oxidation in the vicinity of the film surface, and hydrogenation in the deeper regions of the film. These results suggested that H_2O annealing could improve the carrier transport properties by opening up shorter percolation paths, and by increasing the effective carrier mobility and density.

2.5. Single-electron transistors using silicon nanocrystals

The preceding sections have concentrated on SETs fabricated in continuous nc-Si films. In such a film, the GBs are narrow (~ 1 nm) and if the material is heavily doped, the SET has a comparatively moderate resistance (~100 kΩ or greater) outside the Coulomb blockade region. However, we have seen that single-electron charging effects can be overcome thermally by increasing electron delocalisation with temperature. The electrons can be localised far more strongly in a discontinuous nc-Si film with higher potential barriers between the grains. One of the earliest observations of single-electron effects at room temperature was by Yano *et al* [5], in nanowires fabricated in ultra-thin (~ 3 nm), strongly granular, nanocrystalline silicon layers with grains ~1 nm in size (Fig. 14(a)). In these materials, the grains can be separated by gaps of comparable size. Such a system can show strong single electron effects in the *I-V* characteristics even at room temperature. However, the large tunnel gap resistance leads to a low device current, ~ 10 fA. In a similar room temperature SET design, Choi *et al* [65] have used a thin, discontinuous, PECVD deposited film with 8 nm - 10 nm diameter silicon grains. Metal source and drain electrodes separated by a gap of <30 nm were deposited on top of the film and used to apply a voltage across the grains.

Silicon nanocrystals provide a means to form precisely the SET islands using growth techniques. A very promising technique for this purpose is to grow the silicon nanocrystals using plasma decomposition of SiH_4, e.g. ~ 8 nm ± 1 nm size crystals with a surface oxide ~1.5 nm thick can be prepared [7, 8]. A number of different configurations of SET designs are possible using these techniques [66-69]. These include planar devices where the nanocrystals are deposited on source and drain contacts defined in SOI material, separated by a narrow 30 nm gap (Fig. 14(b)). A top gate supported on a deposited oxide layer is used to control the current. In this configuration, it is possible to observe single-electron charging effects in the device transconductance up to room temperature [68]. An alternative is to deposit the

nanocrystals in a nano-scale hole etched in a silicon dioxide layer, and then top-fill the hole with polycrystalline silicon [69]. This is shown schematically in Fig. 14(c).

2.6. Comparison with crystalline silicon SETs

We observe that while nc-Si nanowire and point-contact SETs (Sec. 2.2 – 2.3) appear to be similar superficially to crystalline Si nanowire SETs [30-35], the mechanism for formation of the tunnel barriers is very different. The tunnel barriers in the nc-Si devices are defined by the GBs. While additional disorder effects associated with the device surface conditions or the non-uniformity of the dopant distribution (the proposed mechanism for crystalline silicon nanowire SETs) can also occur, they are less significant. We have seen that careful preparation of the nc-Si film can be used to control the tunnel barrier properties more accurately. This implies that the active regions of the device, i.e. the grains and GBs within the nanowire or point-contact, can be defined precisely by material processing techniques rather than high-resolution lithography or disorder, and very large numbers of quantum dots can be formed simultaneously over the entire chip area if necessary. Silicon nanocrystals also provide a means for this (Sec. 2.5). Such a process is an extremely attractive alternative to high-resolution lithography at the nanometre-scale over a large area. The SET islands can also be grown or deposited at any convenient stage of the process, greatly increasing in flexibility the fabrication process, e.g. a nc-Si room-temperature SET could be incorporated within the gate of a scaled Si MOSFET to define a room-temperature few-electron random-access memory cell.

3. Electron coupling effects in nanosilicon

It is possible to use the nc-Si point-contact SET to investigate electronic interactions between two or more nanosilicon grains. By varying the dimensions of the point-contact, the number of grains taking part in the single-electron transport process can be varied, and by tailoring the GB selective oxidation process (Sec. 2.4), the strength of the inter-grain electron coupling can be controlled. It is then possible to operate the device at low temperature as a double- or multiple-quantum dot device with electron interactions between the quantum dots formed at the grains.

Electrostatic coupling effects have been investigated in great detail at milli-Kelvin temperatures in double quantum dots formed in GaAs/AlGaAs two-dimensional electron gas (2-DEG) materials (a review may be found in [70]). In these experiments, two gates are used to change the potentials of two quantum dots quasi-independently, and a plot of the Coulomb oscillations v.s. two gate voltages forms hexagonal regions of constant electron number on the quantum dots, associated with single-electron interactions between the dots. This forms a ‘charge stability’ diagram where the total electron number changes by one between neighbouring hexagons. If the quantum dots are strongly tunnel-coupled, then the electron wavefunctions on the two dots can also interact with each other, forming new ‘quasi-molecular’ states, analogous to a covalent bond. Resonant tunnelling through these states leads to additional peaks in the device conductance. These states have been observed near ~50 mK temperature in measurements on GaAs/AlGaAs double quantum dots [71].

We now discuss electron coupling effects in nc-Si point-contact SETs [52, 72]. The devices used point-contacts ~30 nm × 30 nm × 40 nm in size, with two side-gates, and were fabricated in a ~40 nm-thick heavily doped LPCVD film with grain size from ~10 – 30 nm and ~1 nm-thick amorphous Si GBs. Only a few grains existed within the channel at most, and different grains contributed in varying degrees to the device conduction. A scanning electron micrograph of the device is shown in Fig. 15. By modifying the inter-grain coupling by selective oxidation of the GBs, only electrostatic, or combined electrostatic and electron wavefunction coupling effects between two quantum dots could be observed at 4.2 K in the Coulomb oscillation pattern as a function of the two gate voltages. Different grains influenced the Coulomb oscillations in different ways, e.g. a single or two grains could dominate the Coulomb oscillations, or nearby grains could electrostatically switch the oscillations without taking part directly in conduction across the device.

The GB properties in these devices were controlled by varying the duration of the selective oxidation process, and by subsequent argon annealing. If the device was oxidised at 650°C – 750°C, followed by annealing in argon at 1000°C, then this created a high and wide GB tunnel barrier (>100 meV) where electrostatic coupling effects dominated. If the device was oxidised only, without annealing, then the GB tunnel barriers remained low (~40 meV) and narrow and the grains were more strongly coupled. These devices showed both electrostatic and electron wavefunction coupling effects.

3.1. Electrostatic coupling effects

Figure 16(a) shows a three-dimensional grey-scale plot of the drain–source current I_{ds} in a device with electrostatically coupled grains at 4.2 K, as a function of the voltages on gate 1 and gate 2 (V_{g1} and V_{g2} respectively) and V_{ds} = 2 mV. The maximum value of the current (white regions in the plot) is relatively low (I_{ds} = 1.2 pA). A series of lines (marked using dotted lines) are formed by shifts in the Coulomb oscillation positions as a function of both V_{g1} and V_{g2}. These oscillation lines occur when the single-electron energy levels in the point-contact align with the Fermi energy in the source. As both the gates couple to the grain, the energy of a single-electron level relative to the source Fermi energy depends on a linear combination of the two gate voltages. This leads to the oscillation peaks and valleys tracing diagonal lines across the plot. Switching of the position of the oscillation lines is also observed, which implies an abrupt change in the energy of the corresponding single-electron level. The behaviour can be attributed to single-electron charging of a nearby grain, coupled electrostatically to the dominant grain [52].

The characteristics of Fig. 16(a) can be understood using the circuit of Fig. 16(b). The circuit uses a grain (QD1), connected to the source and drain by tunnel junctions T_1 and T_2 and coupled capacitively to the two gates by the capacitors C_{g1} and C_{g4}. A nearby grain (QD2), coupled to QD1 by the tunnel capacitor C_f, can be charged with electrons from the source via tunnel junction T_3. QD2 is also coupled capacitively to the gates. In such an arrangement, the Coulomb oscillations of QD1 form a series of lines as a function of the two gate voltages due to the capacitive coupling of the energy levels of QD1 to both gates. The solid lines in Fig. 16(c) show this schematically. The electron number on QD1 differs by one between regions on either side of a line and this number increases as the gate voltages become more positive.

The lines switch in position when the gate voltages overcome the Coulomb blockade of QD1 and the Coulomb blockade of QD2 (along the dotted lines) simultaneously, i.e. at the intersection of the solid and dotted lines. Here, an electron transfers from the source onto QD2, and this change in charge switches (via C_f) the current through QD1. Note that there is no conduction path from source to drain across QD2. The overlap between the single-electron oscillation lines in the experimental characteristics is a function of the cross capacitances C_{g3} and C_{g4} between the grains and the gates.

3.2. Electron wavefunction coupling effects

In contrast to the device characteristics discussed in Fig. 16, which show only electrostatic coupling effects between grains, additional wavefunction coupling effects can be observed in devices that are oxidised only. In these devices, the GB tunnel barriers remain low and narrow. In a region (Fig. 17(a)) where the Coulomb oscillation lines from two quantum dots QD1 and QD2 (solid and dotted lines respectively) intersect, the corresponding energy levels from each quantum dot are resonant at two points '1' and '2'. With strong coupling between these levels, due to the weak GB tunnel barriers, additional 'quasi-molecular' states can be formed. This is shown schematically in Fig. 17(b).

Khallafallah *et al* [72] have observed the formation of quasi-molecular states at 4.2 K in an nc-Si point-contact SET, oxidised at 750°C for 30 minutes only. In a measurement of the device conductance across a region where the oscillation lines from two QDs intersected, i.e. at the two points '1' and '2' (Fig 17(a)), a set of four peaks was observed. These peaks could be fitted using the sum of four Lorentzian peaks. The position of the peaks, i.e. near the points '1' and '2', where two energy levels in adjacent grains were resonant, and their strongly-coupled nature, suggested that they were quasi-molecular states formed by the delocalisation of the electron wavefunctions over adjacent tunnel coupled grains. By comparison, in devices with oxidation and annealing, electron delocalisation was inhibited because of the higher and wider GB tunnel barriers.

4. Nanosilicon memory

Single-electron effects provide a means to control precisely small amounts of charge down to a single electron, raising the possibility of single- or few-electron memory circuits with high potential for scaling. In these memories, either the Coulomb blockade effect in a SET is used to trap electrons on a storage capacitor or the capacitor is scaled to an extent that only single or a small number of electrons can be stored on it. Following the early development of single-electron memory using MTJs defined in GaAs delta doped layers [19], other memories cells were demonstrated in both crystalline SOI [73-76] and nanosilicon materials. In the following, we introduce nanosilicon few-electron memory cells.

There has been considerable interest in the development of few-electron memory cells using silicon nanocrystals to store charge (5, 6, 77-83). A number of these memory cells [6, 77-81] are analogues of non-volatile 'FLASH' memory cells, where the charge is stored on a 'floating-gate' formed by a discontinuous layer of silicon nanocrystals. Figure 18(a) shows a schematic diagram of such a memory cell. The

silicon nanocrystals can be grown in silicon–rich oxide, by direct seeding on an oxide, by high-density silicon ion-implantation into an oxide, or by plasma decomposition of SiH_4. The nanocrystals are sandwiched in the gate-stack of a silicon MOSFET, separated from the channel by a thin layer of oxide and from the gate by an additional, thicker layer of oxide. Charge can be injected into the nanocrystals by direct tunnelling from the channel across the thin oxide, using a large voltage on the gate. This charge can be sensed by a shift in the threshold voltage of the MOSFET.

In conventional FLASH memory cells, a thicker oxide layer is used above the channel and a high voltage is necessary to transfer electrons on to the gate by Fowler-Nordheim tunnelling or by hot-electron injection. The high electric field and current in the Fowler-Nordheim tunnelling process degrades the oxide over numerous operation of the cell by generating traps, leading to an increasing leakage current which limits the lifetime of the memory. The problem becomes even more severe in a scaled FLASH memory cell, where the stored charge is small and any leakage path quickly discharges the stored charge. In a nanocrystal memory cell, the electric field can be smaller and any leakage paths affect only a small number of nanocrystals. Charge is retained in the remaining nanocrystals and it is less easy to fully discharge the cell. A typical example of such a memory cell, fabricated by Hanafi *et al* [78], uses 3 nm diameter silicon nanocrystals at a density of 1×10^{12} / cm^3. The nanocrystals are separated from each other by ~7 nm and the lower oxide layer is ~1 nm thick. If a charge corresponding to one electron per nanocrystal is stored, then the threshold voltage shifts by 0.35 V, which can change the underlying MOSFET threshold current by 4-5 orders of magnitude. The retention time of such a memory cell can be $\sim 10^5$ s. In alternative designs [77], where the nanocrystals are created by plasma decomposition of SiH_4, the nanocrystal size can also be well controlled.

Single-electron charging and quantum-confinement effects can influence the electric field at which electrons are injected into the nanocrystals. These effects also lead to the stored electrons being separated in energy, providing a means to operate the cell with a precise number of electrons by controlling the magnitude of the writing voltage. These effects can be observed more clearly in highly scaled analogues of discontinuous gate FLASH memories [82, 83], where only a single silicon nanocrystal defines the floating-gate. This nanocrystal is defined by using high-resolution lithography to fabricate a nano-scale silicon island in a polycrystalline silicon layer, deposited on the gate oxide of a nano-scale MOSFET (Fig. 18(b)). Such a memory cell can show discrete charging steps in the MOSFET current as a function of the gate voltage, where each step corresponds to the addition of single electrons onto the nanocrystal. The cell can then be operated with a precisely known number of electrons, down to a single electron. The write time can be less than 1 μs and the retention time can be as long as 5 s at room temperature.

In contrast to these FLASH type memories, Yano *et al* have used their room-temperature SET [5], fabricated in an ultra-thin, strongly granular and non-uniform (~3 nm) nc-Si layer (Fig. 14(a)), as the basis of a prototype 128 Mbit memory operating at room temperature [4]. Memory operation occurs due to the tunnelling of single or small numbers of electrons on to storage nodes formed by the grains in the nanocrystalline silicon layer. The write-erase times are ~10 μs and the retention time is up to one month.

References

[1] Grom, G. F., Lockwood, D. J., McCaffery, J. P., Labbe, N. J., Fauchet, P. M., White Jr, B., Diener, J., Kovalev, D., Koch, F., and Tsybeskov, L., Nature **407**, 358 (2000).

[2] Wilson, W. L., Szajowski, P. F., and Brus, L. E., Science **262**, 1242 (1993).

[3] Littau, K. A., Szajowski, P. F., Muller, A. J., Kortan, A. R., and Brus, L. E., J. Phys. Chem. **97**, 1224 (1993).

[4] Yano, K., Ishii, T., Sano, T., Mine, T., Murai, F., Hashimoto, T., Kobayashi, T., Kure, T., and Seki, K., Proceedings of the IEEE **87**, 633 (1999).

[5] Yano, K., Ishii, T., Sano, T., Hashimoto, T., Kobayashi, T., Murai, F., and Seki, K., Appl. Phys. Lett. **67**, 828 (1995).

[6] Tiwari, S., Hanafi, H., Hartstein, A., Crabbé, E. F., and Chan, K., Appl. Phys. Lett. **68**, 1377 (1996).

[7] Oda, S. and Otobe, M., Mater. Res. Soc. Symp. Proc. **358**, 721 (1995).

[8] Otobe, M., Kanai, T., and Oda, S., Mater. Res. Soc. Symp. Proc. **377**, 51 (1995).

[9] Nakajima, A., Sugita, Y., Kawamura, K., Tomita, H., and Yokoyama, N., J. Appl. Phys. **80**, 4006 (1996).

[10] Kamiya, T., Nakahata, K., Ro, K., Fortmann, C. M., and Shimuzu, I., Mater. Res. Soc. Symp. Proc. **557**, 513 (1999).

[11] Kamiya, T., Nakahata, K., Tan, Y. T., Durrani, Z. A. K., Shimuzu, I., J. Appl. Phys. **89**, 6265 (2001).

[12] Nakahata, K., Ro, K., Suemasu, A., Kamiya, T., Fortmann, C. M., and Shimuzu, I., Jpn. J. Appl. Phys. Pt. 1 **39**, 3294 (2000).

[13] Grabert, H. and Devoret, M. H. (Eds.), *Single Charge Tunneling – Coulomb Blockade Phenomena in Nanostructures*, NATO ASI Series B, Plenum Press, (1991).

[14] Ferry, D. K., *Transport in Nanostructures*, Cambridge University Press, New York, (1996).

[15] Likharev, K. K., Proceedings of the IEEE **87**, 606 (1999).

[16] Meirav, U. and Foxman, E. B., Semicond. Sci. Technol. **10**, 255 (1995).

[17] Ahmed, H., J. Vac. Sci. Technol. B **15**, 2101 (1997).

[18] International Technology Roadmap for Semiconductors (2005)

[19] Nakazato, K., Blaikie, R. J., Cleaver, J. R. A., and Ahmed, H., Electronics Letters **29**, 384 (1993).

[20] Prince, B., *Semiconductor Memories*, 2nd Edition, John Wiley and Sons, New York (1996).

[21] Wong, H. P., Frank, D. J., Solomon, P. M., Wann, C. H. J., and Welser, J. J., Proceedings of the IEEE **87**, 537 (1999).

[22] Nakazato, K., Itoh, K., Sakata, T., Mizuta, H., Ahmed, H., Kisu, T., Kato**,** M., ISSCC2000, 132 (2000).

[23] Tan, Y. T., Kamiya, T., Durrani, Z. A. K., and Ahmed, H., J. Appl. Phys., **94**, 633 (2003).

[24] Kastner, M. A., Phys. Today **46**, 24 (1993).

[25] Kowenhoven, L. P., Marcus, C. M., McEuen, P. L., Tarucha, S., Westervelt, R. M., and Wingreen, N. S., *Mesoscopic Electron Transport*, L. L. Sohn *et al*. (Ed.), Kulwer Academic Press (1997).

[26] Fulton, T. A., and Dolan, G. L., Phys. Rev. Lett. **59**, 109 (1987).

[27] Scott-Thomas, J. H. F., Field, S. B., Kastner, M. A., Smith, H. I., and Antoniadis, D. A., Phys. Rev. Lett. **62**, 583 (1989).

[28] Van Houten, H., and Beenakker, C. W. J., Phys. Rev. Lett. **63**, 1893 (1989).
[29] Paul, D. J., Cleaver, J. R. A., Ahmed, H., and Whall, T. E., Appl. Phys. Lett. **63**, 631 (1993).
[30] Ali, D., and Ahmed, H., Appl. Phys. Lett. **64**, 2119 (1994).
[31] Zhuang, L., Guo, L., and Chou, S. Y., Appl. Phys. Lett. **72**, 1205 (1998).
[32] Takahashi, Y., Namatsu, H., Kurihara, K., Iwadate, K., Nagase, M., and Murase, K., IEEE Trans. Electron Devices **43**, 1213 (1996).
[33] Ishikuro, H., Fujii, T., Saraya, T., Hashiguchi, G., Hiramoto, T., and Ikoma, T., Appl. Phys. Lett. **68**, 3585 (1996).
[34] Smith, R. A., and Ahmed, H., J. Appl. Phys. **81**, 2699 (1997).
[35] Ishikuro, H. and Hiramoto, T., Appl. Phys. Lett. **74**, 1126 (1999).
[36] Müller, H. O., Williams, D. A., Mizuta, H., Durrani, Z. A. K., Irvine, A. C., and Ahmed, H., Physica B **272**, 85 (1999).
[37] Kamins, T. I., J. Appl. Phys. **42**, 4357 (1971).
[38] Seto, J. Y. W., J. Appl. Phys. **46**, 5247 (1975).
[39] Baccarani, G., Ricco, B., and Spandini, G., J. Appl. Phys. **49**, 5565 (1978).
[40] Levinson, J., Shepard, F. R., Scanlon, P. J., Westwood, W. D., Este, G., and Rider, M., J. Appl. Phys. **53**, 1193 (1982).
[41] Cower M. E. and Sedgwick, T. O., J. Electrochem. Soc. **119**, 1565 (1972).
[42] Fripp, A. L., J. Appl. Phys. **46**, 1240 (1975).
[43] Kamins T. I. and Pianetta, P. A., IEEE Electron Dev. Lett. **1**, 214 (1980).
[44] Tringe J. W. and Plummer, J. D., J. Appl. Phys. **87**, 7913 (2000).
[45] Shklovskii, B. I. and Efros, A. L., *Electronic Properties of Doped Semiconductors*, Springer, Berlin (1984).
[46] Dong, Y., Wang, C., Wehrenberg, B. L., and Guyot-Sionnest, P., Phys. Rev. Lett. **92**, 216802 (2004).
[47] Furuta, Y., Mizuta, H., Nakazato, K., Tan, Y. T., Kamiya, T., Durrani, Z. A. K., Ahmed, H., and Taniguchi, K., Jpn. J. Appl. Phys. **40**, L615 (2001).
[48] Furuta, Y., Mizuta, H., Nakazato, K., Kamiya, T., Tan, Y. T., Durrani, Z. A. K., and Taniguchi, K., Jpn. J. Appl. Phys. **41**, 2675 (2002).
[49] Irvine, A. C., Durrani, Z. A. K., Ahmed, H., and Biesemans, S., Appl. Phys. Lett. **73**, 1113 (1998).
[50] Tan, Y. T., Durrani, Z. A. K., and Ahmed, H., J. Appl. Phys. **89**, 1262 (2001).
[51] Furuta, Y., Mizuta, H., Nakazato, K., Kamiya, T., Tan, Y. T., Durrani, Z. A. K., and Taniguchi, K., Jpn. J. Appl. Phys. **41**, 2675 (2002).
[52] Khalafalla, M. A. H., Mizuta, H., and Durrani, Z. A. K, IEEE Trans. on Nanoelectronics **2**, 271 (2003).
[53] Tan, Y. T., Kamiya, T., Durrani, Z. A. K., and Ahmed, H., Appl. Phys. Lett. **78**, 1083 (2001).
[54] Tan, Y. T., Durrani, Z. A. K., and Ahmed, H. J. Appl. Phys. **89**, 1262 (2001).
[55] Durrani, Z. A. K., Kamiya, T., Tan, Y. T., and Ahmed, H., Microelectronics Engineering **63**, 267 (2002).
[56] Durrani, Z. A. K., Physica E **17**, 572 (2003).
[57] Y. Kanemitsu, Phys. Rep. **263**, 1 (1995).
[58] Kanemitsu, Y., Okamoto, S., Otobe M., and Oda, S., Phys. Rev. B **55**, 7375 (1997).
[59] Brus, L. E., Szajowski, P. F., Wilson, W. L., Haris, T. D., Shuppler, S., and Citrin, P. H., J. Am. Chem. Soc. **117**, 2915 (1995).
[60] Natori, K., Uehara T., and Sano, N., Jpn. J. Appl. Phys. **39**, 2550 (2000).

[61] Pooley, D. M., Ahmed, H., Mizuta, H., and Nakazato, K., Appl. Phys. Lett. **74**, 2191 (1999).
[62] Mizuta, H., Wagner, M., and Nakazato, K., IEEE Trans. Electron Devices **48**, 1103 (2001).
[63] Kamiya, T., Durrani, Z. A. K., and Ahmed, H., Appl. Phys. Lett. **81**, 2388 (2002).
[64] Kamiya, T., Durrani, Z. A. K., Ahmed, H., Sameshima, T., Furuta, Y., Mizuta, H., and Lloyd, N., J. Vac. Sci. and Tech. B **21**, 1000 (2003).
[65] Choi B. H., Hwang, S. W., Kim, I. G., Shin, H. C., Kim, Y., and Kim, E. K., Appl. Phys. Lett. **73**, 3129 (1998).
[66] Dutta, A., Kimura, M., Honda, Y., Otobe, M., Itoh, A. and Oda, S., Jpn. J. Appl. Phys. **36,** 4038 (1997).
[67] A. Dutta, S. P. Lee, Y. Hayafune, S. Hatatani and S. Oda, Jpn. J. Appl. Phys. **39**, (2000) 264.
[68] A. Dutta, S. Oda, Y. Fu, and M. Willander, Jpn. J. Appl. Phys. **39**, 4647 (2000).
[69] Nishiguchi K. and Oda, S., J. Appl. Phys., **88**, 4186 (2000).
[70] Van der Wiel, W. G., De Franceschi, S., Elzerman, J. M., Kouwenhoven, L. P., Fujisawa, T., and Tarucha, S., Rev. Mod. Phys. **75**, 1 (2003).
[71] Blick, R. H., Pfannkuche, D., Haug, R. J., v. Klitzing, K., and Eberl, K., Phys. Rev. Lett. **80**, 4032 (1998).
[72] Khalafalla, M. A. H., Durrani, Z. A. K., Mizuta, H., Appl. Phys. Lett. **85**, 2262 (2004).
[73] Stone, N. and Ahmed, H. Appl. Phys. Lett. **73**, 2134 (1998).
[74] Durrani, Z. A. K., Irvine, A. C., Ahmed, H., and Nakazato, K., Appl. Phys. Lett. **74**, 1293 (1999).
[75] Irvine, A. C., Durrani, Z. A. K., and Ahmed, H., J. Appl. Phys. **87**, 8594 (2000).
[76] Durrani, Z. A. K., Irvine, A. C., and Ahmed, H., IEEE Trans. on Electron Devices **47**, 2334 (2000).
[77] Hinds, B. J., Nishiguchi, K., Dutta, A., Yamanaka, T., Hatanani, S., and Oda, S., Jap. J. Appl. Phys. **39**, 4637 (2000).
[78] Hanafi, H. I., Tiwari, S., and Khan, I., IEEE Trans. Electron Devices, **43**, 1553 (1996).
[79] Normand, P., Kapetanakis, E., Dimitrakis, P., Tsoukalas, D., Beltsios, K., Cherkashin, N., Bonafos, C., Benassayag, G., Coffin, H., Claverie A., Soncini V., Agarwal A., and Ameen M., Appl. Phys. Lett. **83**, 168 (2003).
[80] Tiwari, S., Rana, F., Chan, K., Shi, L., and Hanafi, H., Appl. Phys. Lett. **69**, 1232 (1996).
[81] Kim, I., Han, S., Han, K., Lee, J., and Shin, H., IEEE Electron Device Lett. **20**, 630 (1999).
[82] Welser, J. J., Tiwari, S., Rishton, S., Lee, K. Y., and Lee, Y., IEEE Electron Device Lett. **18**, 278 (1997).
[83] Guo, L. J., Leobung, E., and Chou, S. Y., Appl. Phys. Lett. **70**, 850 (1997).

Figure captions:

Figure 1. Single-island, double tunnel junction. (a) Schematic diagram. (b) Circuit diagram.

Figure 2. (a) Single-electron energy levels in a double tunnel junction. (b) Coulomb blockade *I*-*V* characteristics.

Figure 3. (a) Single-electron transistor (SET). (b) Single-electron current oscillations in a SET.

Figure 4. Charge stability diagram of a SET.

Figure 5. Energy bands in a one-dimensional chain of *n*-type nanocrystalline silicon grains. (a) Schematic diagram, with a grain isolated by grain boundaries. (b) Charge distribution. (c) Energy bands across the grain and grain boundaries.

Figure 6. Arrenhius plot (shown schematically) of conductance *G* v.s. inverse temperature 1/*T* in nanocrystalline silicon.

Figure 7. (a) Nanowire SET. (b) Scanning electron micrograph of nanowire SET.

Figure 8. Electrical characteristics of a nanocrystalline silicon nanowire SET at 4.2 K. (a) I_{ds}-V_{ds} characteristics. The curves are offset 4 nA / 40mV gate step for clarity. (b) I_{ds}-V_{gs} characteristics.

Figure 9. Nanocrystalline silicon point-contact SET. (a) Schematic diagram. (b) Transmission electron micrograph of the nanocrystalline silicon film. (c) Scanning electron micrograph of a device.

Figure 10. Arrenhius plot of conductivity v.s. inverse temperature in nanocrystalline silicon point-contact SET, for V_{ds} = 50 mV > V_{cg}, and V_{ds} = 0 V < V_{cg}. Here V_{cg} ~ 10 mV.

Figure 11. Scanning electron micrograph of a nanocrystalline silicon point-contact SET with grain-boundary oxidation, for room temperature operation of the device.

Figure 12. Electrical characteristics of a nanocrystalline silicon point-contact SET with oxidised grain boundaries (a) Temperature dependence of I_{ds}-V_{gs} oscillations. The oscillations persist to 300 K. (b) I_{ds}-V_{ds} characteristics at 300 K.

Figure 13. Schematic diagram of grain boundary oxidation in a nanocrystalline silicon point-contact.

Figure 14. Single-electron transistors using silicon nanocrystals (a) Device using an ultra-thin nanocrystalline silicon film [5]. (b) Device using deposited nanocrystals [68]. (c) Vertical transport device with deposited nanocrystals [69].

Figure 15. Scanning electron micrograph of a nanocrystalline silicon point-contact transistor for the measurement of electron-coupling effects.

Figure 16. Electrostatic coupling effects in a nanocrystalline silicon point-contact. (a) Grey-scale plot of the current at 4.2 K, as a function of two gate voltages. V_{ds} = 2mV and the maximum value of I_{ds} = 1 nA (white). (b) Double quantum-dot model. (c) Schematic of Coulomb oscillation lines.

Figure 17. Electron wave-function coupling effects in a nanocrystalline silicon point-contact. (a) Resonance (at points '1' and '2') between energy levels on two quantum dots, in a plot of the Coulomb oscillations v.s. the gate voltages V_{g1} and V_{g2}. (b) Quasi-molecular states.

Figure 18. Nanosilicon memory cells. (a) Silicon nanocrystal memory cell. (b) Memory cell with a single nano-scale storage node.

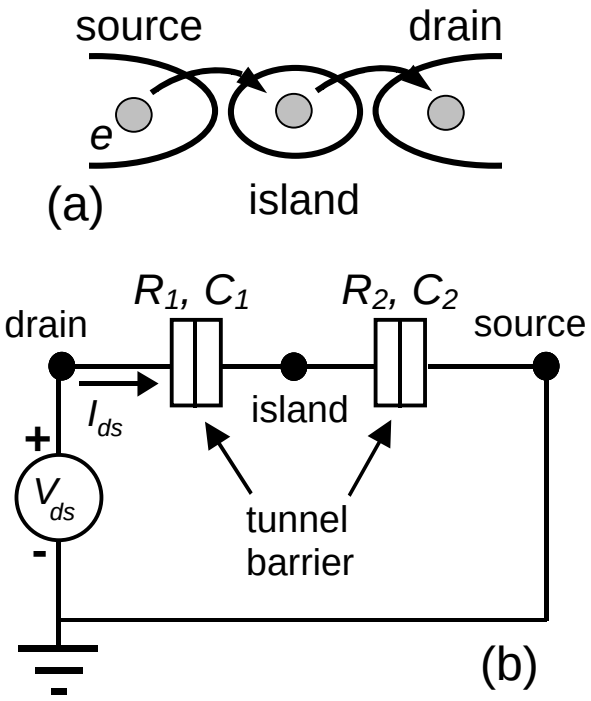
source
drain
e
(a)
island
R1, C1
R2, C2
drain
source
Ids
island
+
Vds
-
tunnel
barrier
(b)

Figure 1

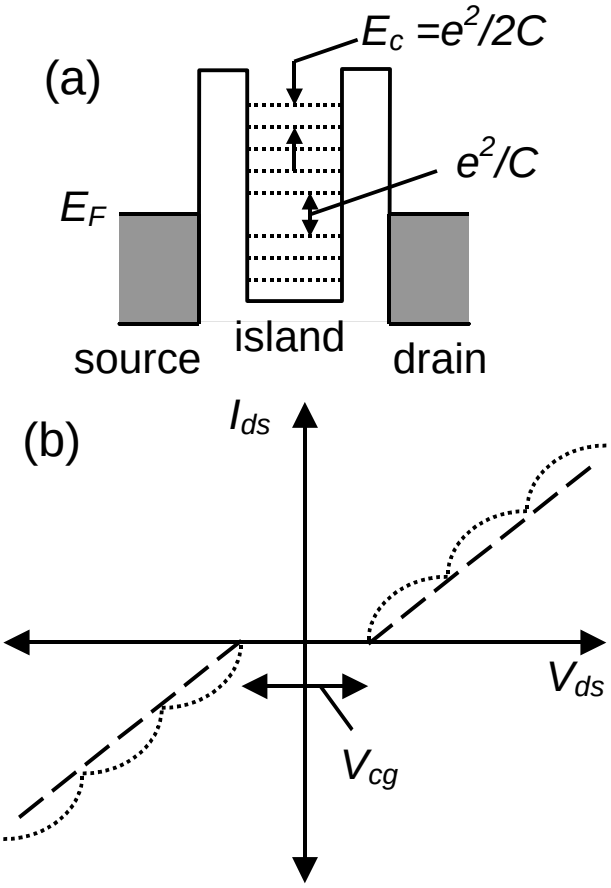

Figure 2

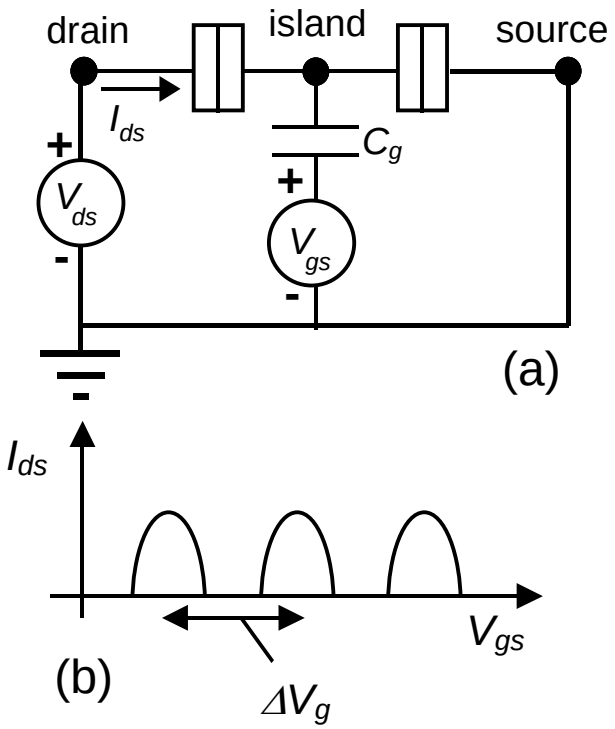

Figure 3

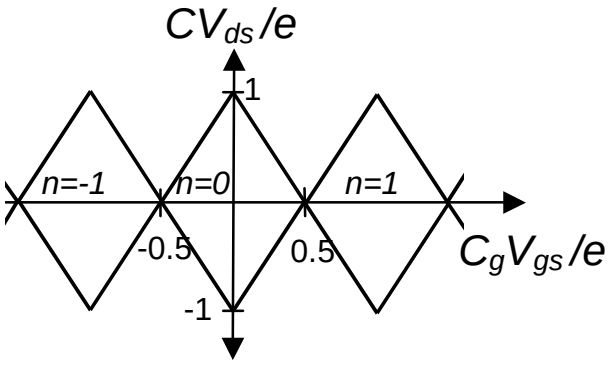

Figure 4

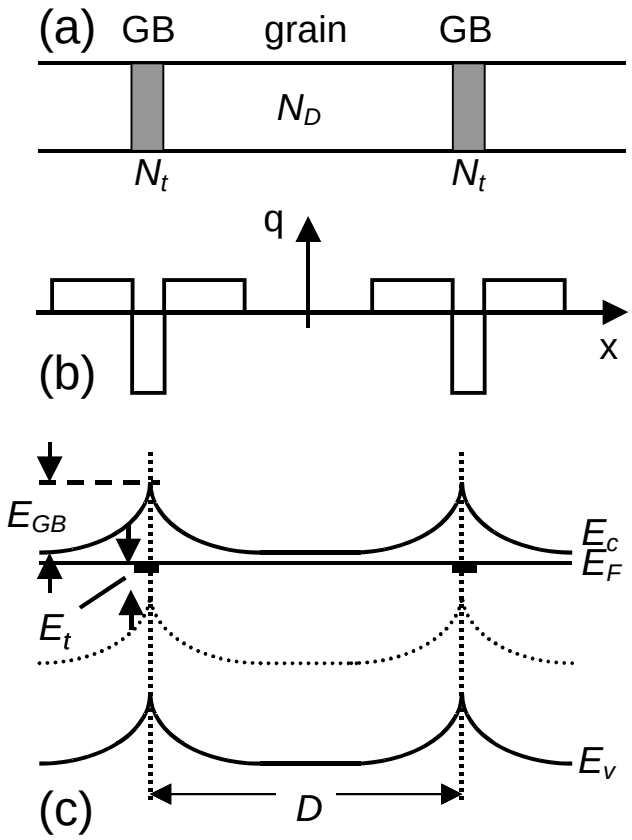

Figure 5

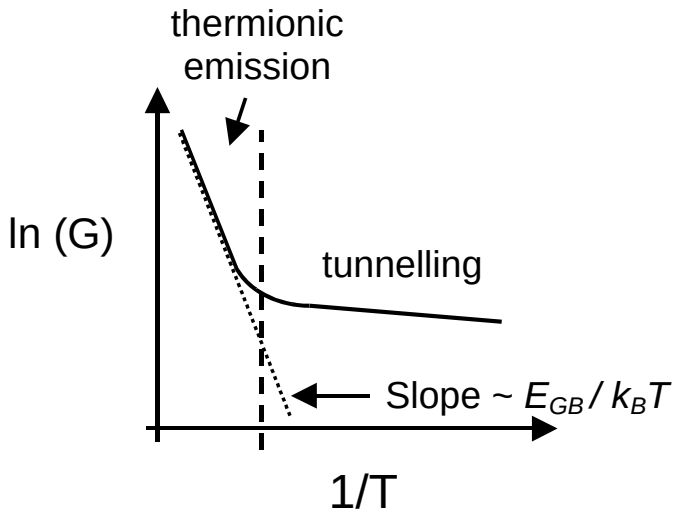

Figure 6

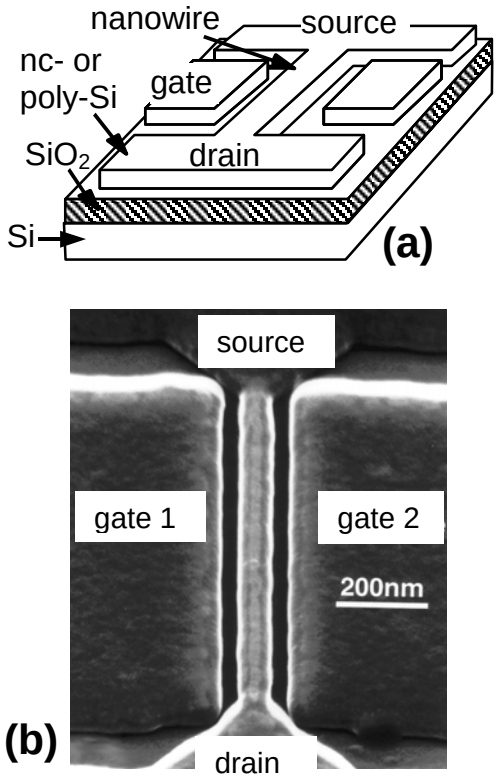
nanowire
source
nc- or
poly-Si
gate
SiO_2
drain
Si
(a)
source
gate 1
gate 2
200nm
(b)
drain

Figure 7

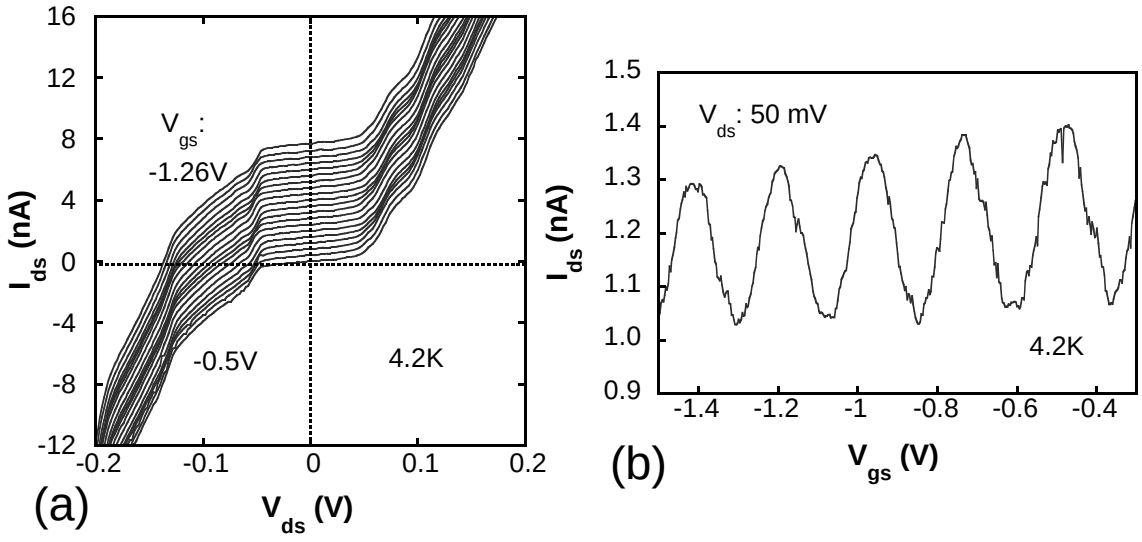
16
12
8
4
0
-4
-8
-12
I_{ds} (nA)
V_{gs}:
-1.26V
-0.5V
4.2K
-0.2
-0.1
0
0.1
0.2
V_{ds} (V)
(a)
1.5
1.4
1.3
1.2
1.1
1.0
0.9
I_{ds} (nA)
V_{ds}: 50 mV
4.2K
-1.4
-1.2
-1
-0.8
-0.6
-0.4
V_{gs} (V)
(b)

Figure 8

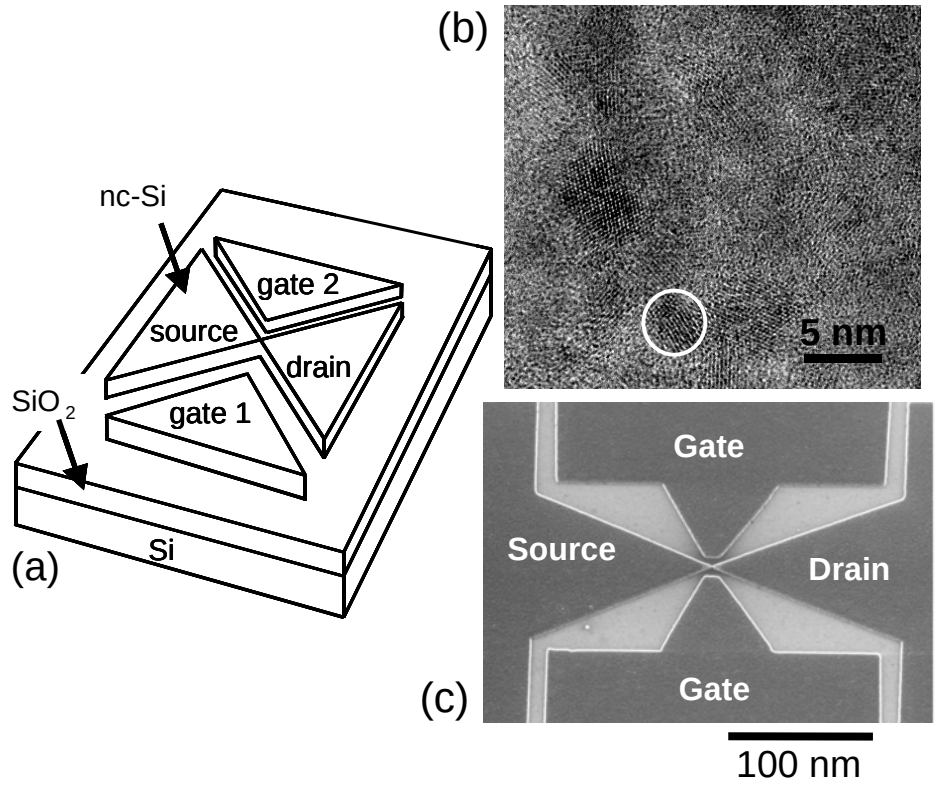
(b)
5 nm
nc-Si
gate 2
source
drain
SiO 2
gate 1
Si
(a)
Gate
Source
Drain
Gate
(c)
100 nm

Figure 9

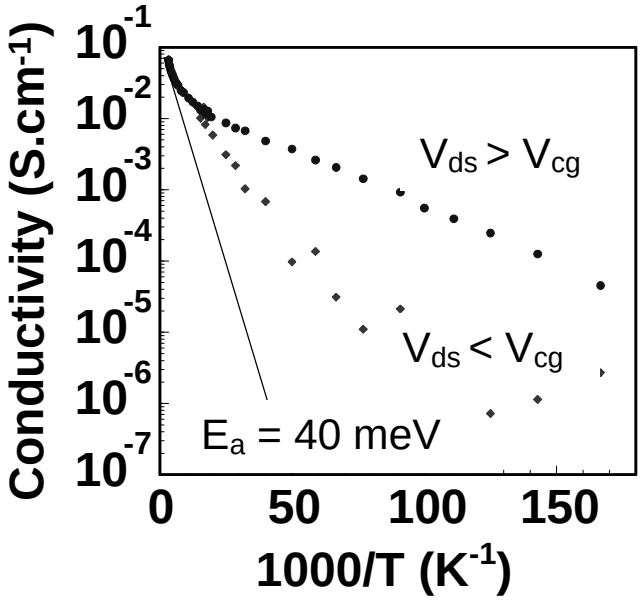
Conductivity (S.cm-1)
10-1
10-2
10-3
10-4
10-5
10-6
10-7
Vds > Vcg
Vds < Vcg
Ea = 40 meV
0
50
100
150
1000/T (K-1)

Figure 10

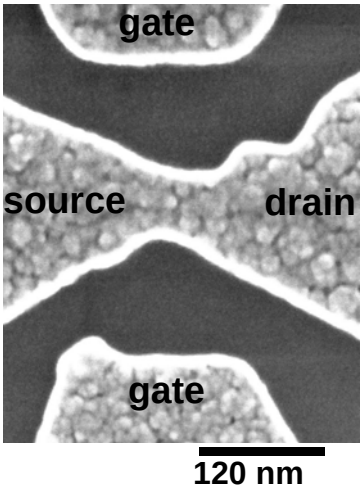

Figure 11

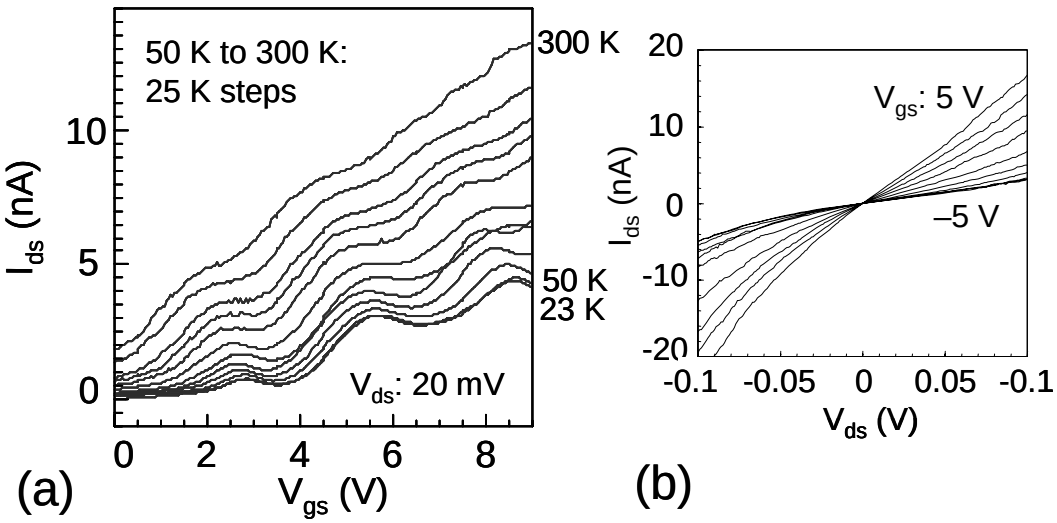
50 K to 300 K:
25 K steps
300 K
50 K
23 K
V_{ds}: 20 mV
I_{ds} (nA)
V_{gs} (V)
(a)
V_{gs}: 5 V
–5 V
I_{ds} (nA)
V_{ds} (V)
(b)

Figure 12

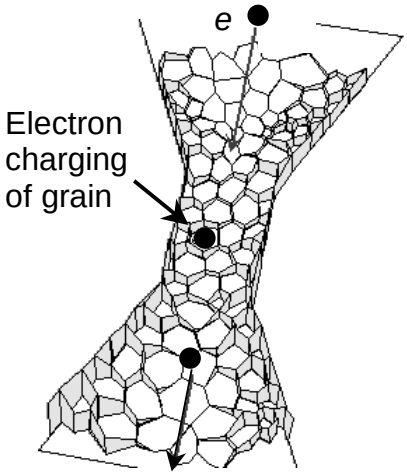

Figure 13

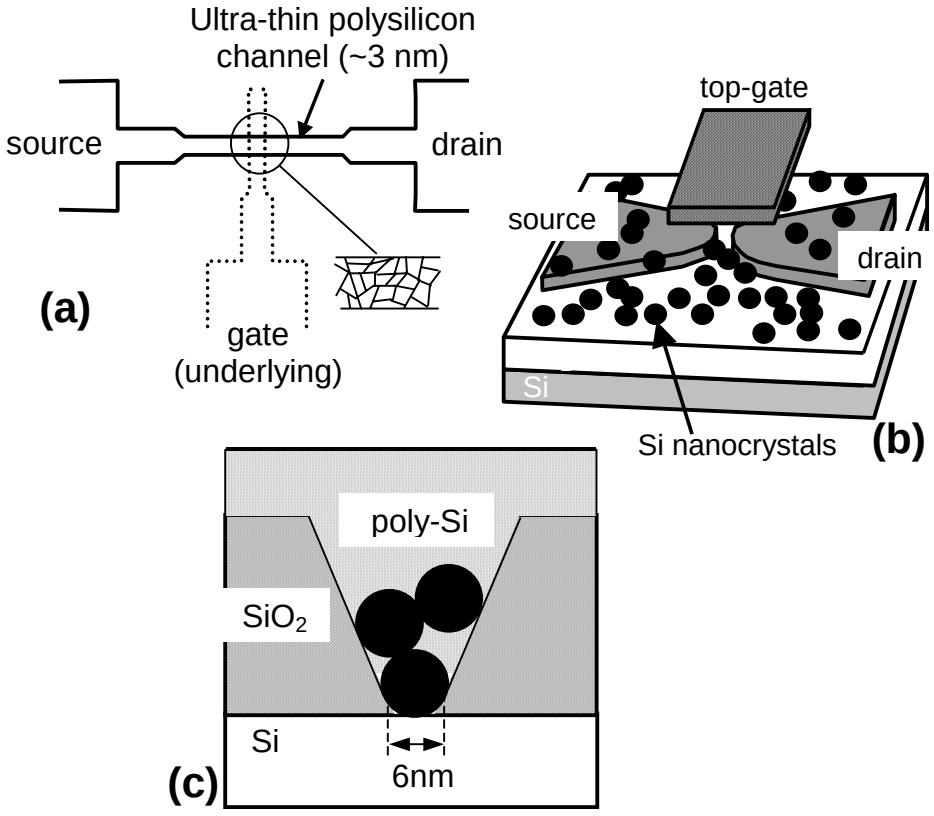
Ultra-thin polysilicon
channel (~3 nm)
source
drain
(a)
gate
(underlying)
top-gate
source
drain
Si
Si nanocrystals
(b)
poly-Si
SiO2
Si
6nm
(c)

Figure 14

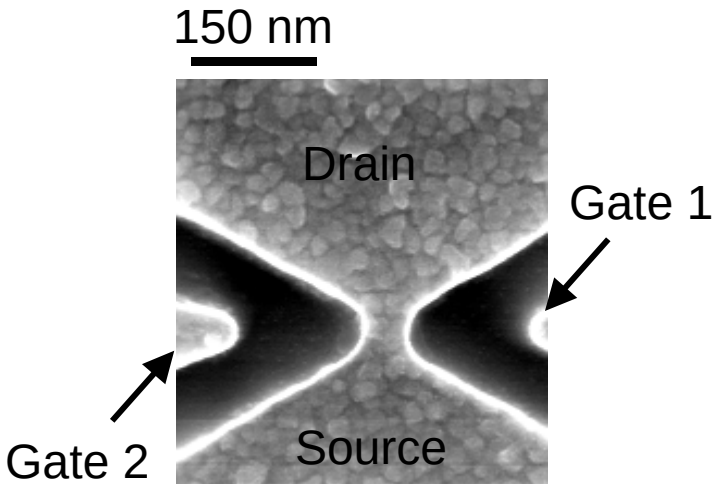

Figure 15

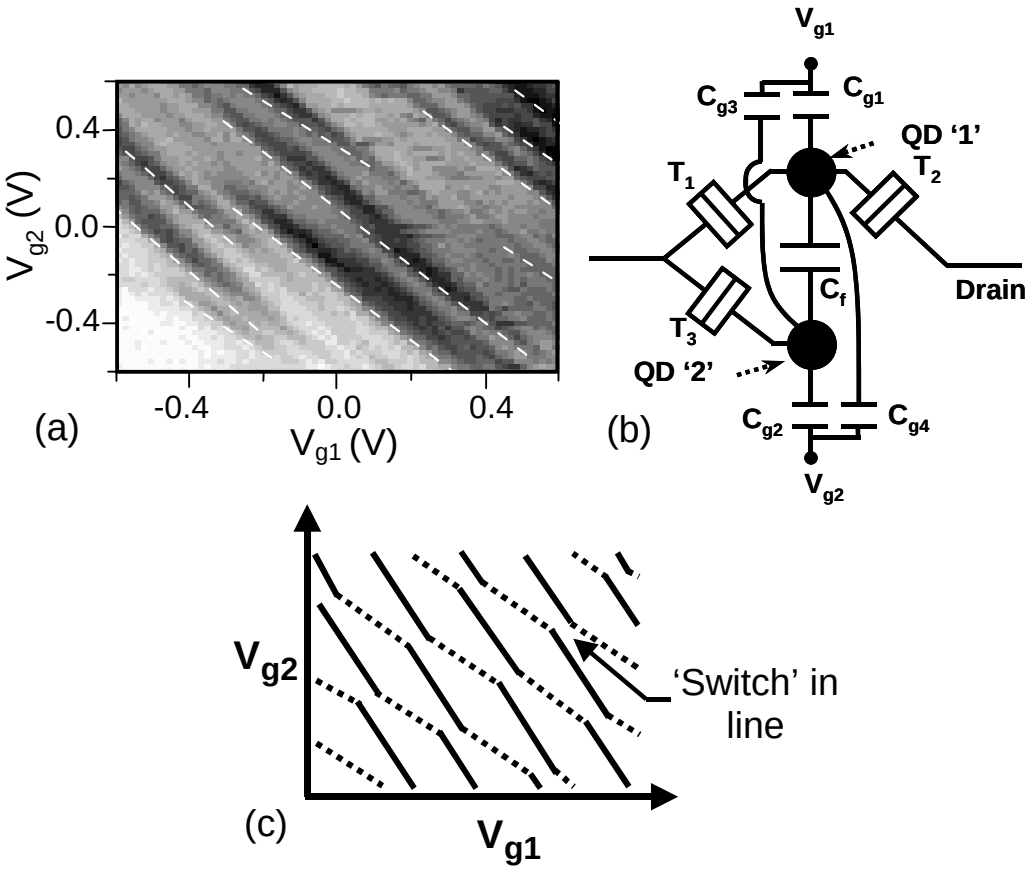
0.4
0.0
-0.4
V_{g2} (V)
-0.4
0.0
0.4
V_{g1} (V)
(a)
V_{g1}
C_{g3}
C_{g1}
QD '1'
T_1
T_2
C_f
Drain
T_3
QD '2'
C_{g2}
C_{g4}
V_{g2}
(b)
V_{g2}
'Switch' in line
(c)
V_{g1}

Figure 16

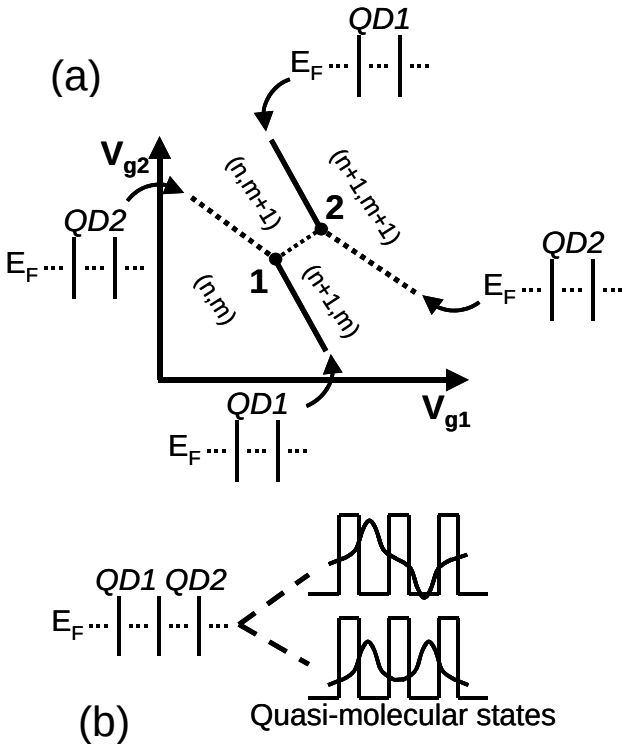
(a)
QD1
E_F
V_g2
QD2
E_F
(n,m+1)
(n+1,m+1)
2
1
(n,m)
(n+1,m)
QD2
E_F
QD1
E_F
V_g1
QD1 QD2
E_F
(b)
Quasi-molecular states

Figure 17

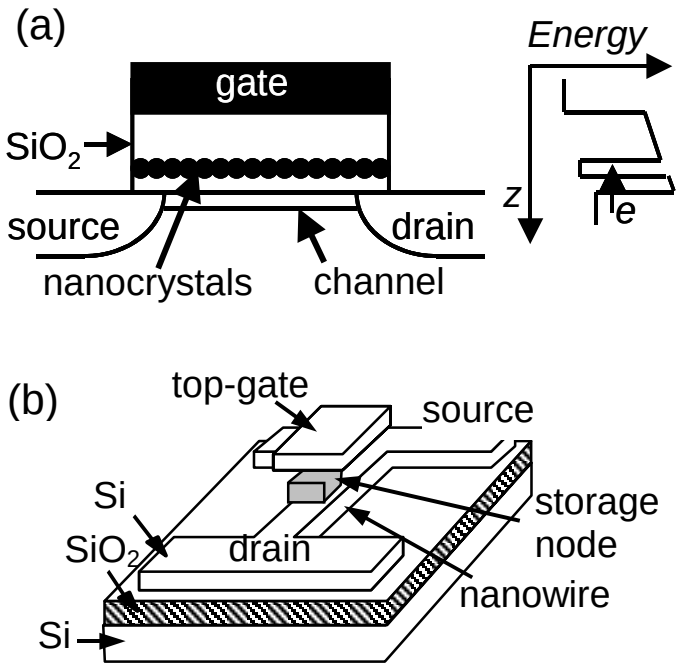
(a)
Energy
gate
SiO2
source
drain
z
e
nanocrystals
channel
(b)
top-gate
source
Si
storage
node
SiO2
drain
nanowire
Si

Figure 18