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Study of MOS-gated strained-Si buried channel Field Effect Transistors

K. Fobelets[1], J.E. Velazquez-Perez[2], and T. Hackbarth[3]

[1]Department of Electrical and Electronic Engineering, Imperial College London, Exhibition Road, SW7 2BT London, UK
[2]Departemento de Fisica Aplicada, Universidad de Salamanca, Edificio Trilingüe, Pza. de la Merced s/n, 37008 Salamanca, Spain
[3]Daimler-Chrysler AG, Research Center Ulm, Wilhelm-Runge-St. 11, 89081 Ulm, Germany

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Abstract *MOS-gated strained-Si modulation doped Field Effect Transistors (MOSMODFETs) traditionally suffer from parallel conduction causing degradation of the device performance below that of the Si control fabricated in the same batch. We present a MOSMODFET in which parallel conduction is avoided through the use of ultra-thin modulation doped layers and TMAH etching to remove the top Si parasitic layer. A low thermal budget and deposited oxides are used to conserve material integrity. This approach has lead to MOSMODFETs that show RF performance improvement over the Si control MOSFET and improved DC operation over a temperature range from 10K to 300K. The influence of the low temperature processing on the characteristics is an increase from 0.3 to 1.2 Ω mm of the contact resistance, and the deposited oxide increases the interface state density.*

I. Introduction

Strained-Si n-channel FETs (s-Si FETs) are considered as a possible solution for improving the performance of Si MOSFETs beyond that reached by scaling only. Strain in the channel can be imposed in two ways, *local strain* via the use of spacer layers with well chosen material composition or *global strain* via the use of graded SiGe buffers, also called virtual substrates [1]. Two different MOS configurations exist in the globally strained approach: s-Si surface channels (s-Si SC) [2,3], these use a thermal oxide for gating and s-Si buried channels (s-Si BC) with a metal Schottky gate [4], equivalent to their III-V HEMT counterpart. Surface channel devices have the advantage of a small gate-to-channel distance but retain the influence of the rough $Si:SiO_2$ interface. SCs have also been found more temperature robust. Buried channels benefit from modulation doping and separation of the channel from the surface (reduction in surface roughness and impurity scattering). This approach needs careful design of the thickness and doping densities of the modulation doped layers in order to avoid parallel conduction. The most successful BC approach is using a Schottky gate to bring the gate as close as possible to the channel [5]. Unfortunately, Schottky gates are relatively leaky for depletion mode devices and increases the off-current and thus the power consumption of the s-Si BC FETs [6], making them less attractive to low power RF performance [7]. Replacing the Schottky gate with a MOS-gate can solve this problem but serious parallel conduction problems together with an important temperature sensitivity of the heterojunction quality have hindered progress in this field [8]. Lately the surface channel devices are gaining in popularity because their relative ease of growth, better tolerance to processing temperatures, and similarity to the classical MOSFET. However for applications where high speed at low power levels is needed, buried channel devices might be competitive. An early indication of this feature was given by J. Welser in [9], where it is shown that the effective mobility of the carriers in the channel outperform the other MOSFETs at low effective fields. More recently, research on Schottky-gated s-Si BC FETs for low power applications have demonstrated the potential of these devices at low electric fields [10]. In this paper, we suggest an ultra-thin modulation doped layer structure and alternative processing steps to avoid parallel conduction. Deposition of a gate insulator is used to keep the processing temperature low and a 1-step low thermal anneal is used for the implants. The MOS-gated s-Si BC FETs were characterised both at DC (10K to 300K) and RF, which shows their improved performance compared to the Si control MOSFET processed in the same run.

The paper is organised as follows: in section II growth and processing issues are followed by the extraction of contact resistances and interface state density. The DC characterisation is done for three gate lengths: 0.3, 0.5 and 1 μm and includes temperature dependencies, off-currents and backgating sensitivity, presented in section III. In section IV the RF characterisation gives the cut-off frequency and discusses the influence of the gate oxide thickness on the measurements. At each stage, the performance of the s-Si BC device is compared to the Si MOSFET.

II. Device structure and fabrication

The s-Si BC device layers were grown by MBE. The layer structure is given in Table I.

Table I: Layer structure of the strained-Si Buried Channel FET

10 nm Si
3 nm $Si_{0.7}Ge_{0.3}$ n=3 10^{18} cm^{-3}
5 nm 30% i-SiGe
8 nm Si channel (quantum well)
100 nm 30% i-SiGe
1 μm p=5 10^{17} cm^{-3} $Si_{0.7}Ge_{0.3}$
0-30% p=5 10^{17} cm^{-3} graded buffer layer
p-doped Si substrate

The top Si layer is used only to protect the SiGe from oxidation and to allow a full RCA wafer-cleaning step

at the start of processing. In order to make a successful MOS-gated BC FET, it is essential to keep the distance between gate and channel as small as possible. Therefore the supply layer is only 3 nm thick with a sufficiently high doping (Sb is used) to allow an adequate carrier concentration in the channel. Only one supply layer was used in order to avoid leakage currents due to parallel conduction at low voltage levels through the 2nd doped layer underneath the quantum well [11]. For full power high frequency applications, double doping around the quantum well is attractive, for low power operation, top doping only, is preferred. Processing was done in the Microelectronics fabrication facility of the University of Southampton, UK, where the minimal reproducible feature size is 300nm. Immediately before defining the gate oxide, the residual Si cap layer, applied during growth for protection of the SiGe supply layer, is completely removed by a selective TMAH ((CH3) 4NOH) etch [12] preceded by a 20s BHF dip to remove the native oxide of the Si top layer. This selective etch (stops on the heavily doped SiGe supply layer) avoids any parasitic s-Si surface channel that would contributes to conduction from a width of 2 nm upwards [8]. To avoid deterioration of the SiGe layer during processing, no further HF based cleaning was done.

It is well known that Sb and Ge segregates to the surface at relatively low temperatures. Therefore, the gate insulator needs to be deposited at low temperatures. Recently, a large amount of investigations are carried out on high k dielectrics to replace the oxide gate [13]. Although high-k dielectrics would be an option for s-Si BC FETs, research is still in its infancy [14]. To simplify the processing an LPE CVD low temperature oxide, deposited at 400°C, was used. Investigations into the homogeneity of the thickness and leakage through the oxide for oxide thickness of: 5nm < t_{ox} < 40 nm, determined that without further optimisation of the oxide deposition technique a minimum of 20 nm was needed to avoid oxide related yield problems. Therefore it was decided to use a 20nm deposited oxide, notwithstanding the fact that this large thickness will degrade the control of the gate over the channel. Oxide leakage currents were found to be negligible in 90% of the measured devices.

To adhere to the low thermal budget required, the ohmic contact implantations were annealed at only 600°C. This low temperature anneal might lead to un-restored implantation damage and increases the contact resistance as will be discussed later. No silicidation was used to reduce the ohmic contact resistance on none of the device types. This choice was made to remove silicidation related problems on SiGe material under low thermal processing. Source and drain were self-aligned to an in-situ n-doped polySi gate (this avoids poly-Si gate implant anneals).

In order to allow a comparison, two Si controls without epilayer were added. Si control 1 was processed using the full thermal budget (1000°C) and a 3 nm thermal oxide (900°C), while Si control 2 went through exactly the same process as the s-Si BC layer with a 20nm deposited gate oxide and low temperature anneal steps. The Si control wafers are defined on p-type 18-33 Ω/cm resistivity substrates. The surface has a graded B-dose implant punch through stopper.

The contact resistance R_C of the devices is extracted from the DC I_{DS}-V_{DS} characteristics in strong inversion in the triode region (V_{DS}<0.3V) using the technique presented in [6].

The average value of the contact resistance for the s-Si BC FET with low thermal anneal is R_C=1.2 Ω mm compared to R_C=0.3 Ω mm for Si control 1 and R_C=1.1 Ω mm in Si control 2. This increased resistivity of the ohmic contact is thus mainly due to the limited temperature of the implant anneal. However the contact resistance in the s-Si BC FETs tend to be slightly higher than in Si control 2 potentially due to different diffusion mechanisms of the P implant in Si and SiGe [15].

III. DC characteristics

Four-contact (source, bulk, drain and gate), on-wafer-probe measurements were carried out using an Agilent 4155B semiconductor parameter analyser, controlled by a purpose-written VisualBasic application through a GPIB connection. A typical current-voltage characteristic at room temperature and the associated external transconductance is given in Figure 1 for the 300nm gate length devices (s-Si BC and Si control 2).

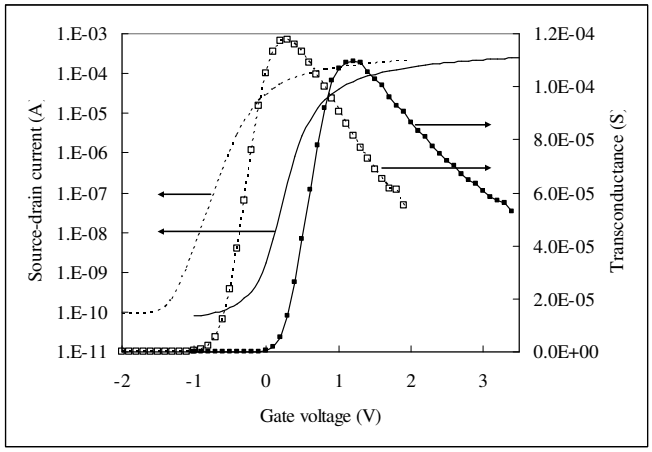


Figure 1: Source-drain current and extrinsic transconductance as a function of gate voltage for the Si MOSFET (full lines) and the SiGe s-Si MOSFET (dashed lines) for a gate length of 300nm and at V_{DS}=0.1V and T=300K.

It is clear that the MOS-gated s-Si BC device outperforms the Si control at DC in the triode region and room temperature. Note that due to the relatively small currents in the triode region, the influence of the increased contact resistance in the s-Si devices is negligible. In order to intrinsic performance of the devices in both, triode and saturation region, the maximum intrinsic transconductance g_{m0}^{max} was calculated using Eq. 1.

$$g_{m0}^{max} = \frac{g_m}{1 - 2g_d R_C - g_m R_C} \quad (1)$$

Where g_m is the extrinsic transconductance, g_d the drain to source conductance at the gate voltage for maximum g_m, and R_C is the contact resistance. The results are

presented in Figure 2. This demonstrates the DC performance improvement of the s-Si MOS-gated buried channel FET over Si control 2 at both low and high drain bias.

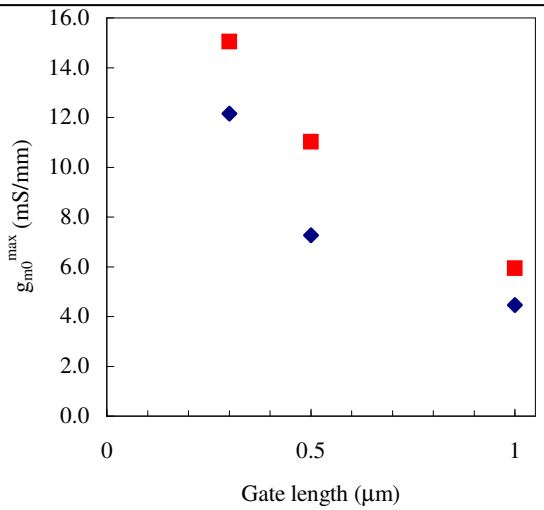
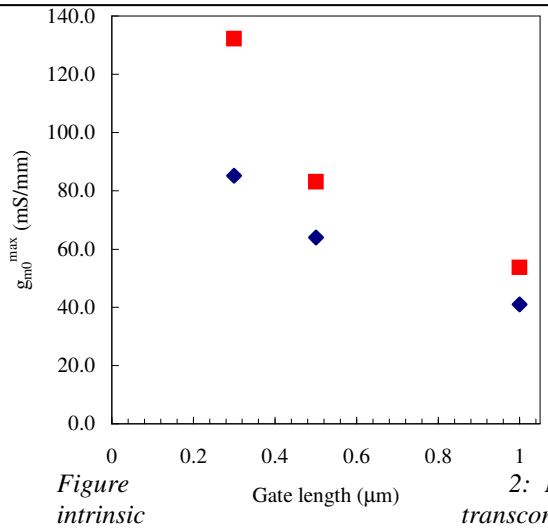


Figure 2: Maximum intrinsic transconductance as a function of gate length.
■ *s-Si BC MOSFET,* ♦ *Si control 2, left:* V_{DS} *= 0.1 V, right:* V_{DS} *= 1 V. The bulk contact is connected to source (ground).*



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Similar devices as those used for the on-wafer room temperature DC measurements where packaged and inserted in a CTI-Cryogenics closed cycle He cryostat with a temperature range between T = 300 K and T = 10 K and a temperature accuracy of less than 1 K during the measurements. The variation of the maximum intrinsic transconductance and the contact resistance as a function of temperature for both Si control 2 and s-Si MOSFET is given in Figure 3. The contact resistance is decreasing monotonically as a function of decreasing temperature due to reduced phonon scattering. It indicates that the devices remain operational down to 10K (no doping freeze-out effects). The transconductance on the other hand increases with decreasing temperature down to a temperature of ±100K and then remains constant for both the Si control and the s-Si BC MOSFETs. The improved mobility in the s-Si MOSFETs compared to the Si control is caused by 1) a reduction in the effective mass of the electrons in the s-Si channel and 2) the splitting of the conduction band by strain that impedes intervalley scattering processes. The performance of both device types first increases with decreasing temperature as the importance of phonon scattering diminishes and then remains constant below a transition temperature of 100K, indicating that the lower average effective mass and the reduced coulomb scattering in the s-Si channel are the remaining improvement factors at low temperatures. These curves are typical for measurements done at low longitudinal electric fields across the FETs. The performance improvement is strongly dependent on both the effective and longitudinal electric field as different scattering processes, some of which independent of temperature, become more important at different effective fields [16].

Current-voltage and high frequency (100kHz) CV measurements done on a fatFET with dimensions 100µm x 250µm at 300K allow to extract the effective mobility of the device following the method proposed in [7]. The maximum values of the effective field mobility are lying in the range of 580 – 700 cm^2/Vs for the s-Si BC device, while between 300 – 400 cm^2/Vs for the Si control 2 at a vertical effective field of ~0.18 MV cm^{-1}. Variations of these values are the result of variations in oxide thickness and layer thickness and doping across the wafer. The effective drift mobility of the s-Si BC MOSFET remains higher than the Si control over the whole range of vertical field values

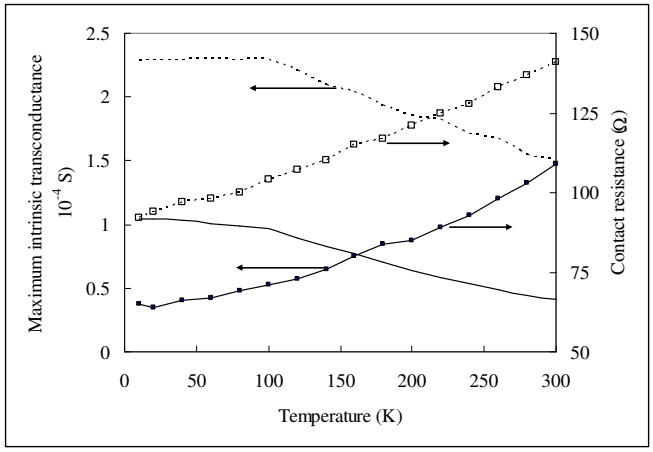

Figure 3: Maximum intrinsic transconductance and contact resistance as a function of temperature for the Si MOSFET (full lines) and the s-SiGe BC MOSFET (dashed lines) for a gate length of 300nm and at V_{DS}*=0.1V*

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To investigate the influence of the deposited oxide on the gating performance, on-transistor split-CV measurements [12] were done using a Wayne Kerr 6440B LCR meter and a measurement frequency of 100kHz. The results, normalised to the oxide thickness t_{ox} are presented in Figure 4.

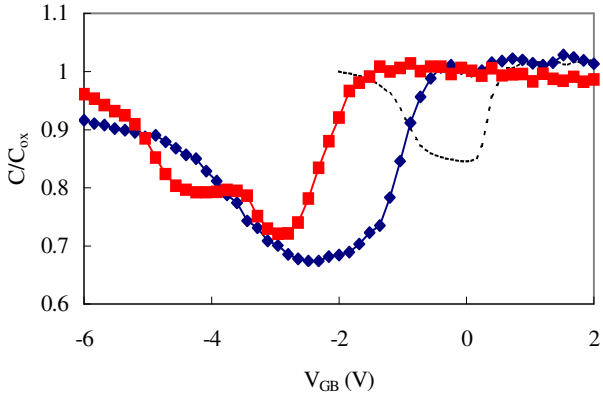

Figure 4: Normalised oxide capacitance as a function of the gate-bulk voltage. The bulk is kept grounded and the DC and AC signal is applied to the gate. ■ s-Si BC MOSFET, ♦ Si control 2 and --- Si control 1.

Comparing Si control 1 and 2, which have the same substrate doping, shows a broader CV dip between accumulation and inversion region in control 2 because of the difference in oxide thickness [17] and stretch-out of the CV curve due to interface states, resulting in a larger V_T shift [18]. The threshold voltage difference between Si control 2 and the s-Si BC FET can also be observed in the DC IV characteristics and is due to the difference in doping (modulation doping) and the energy band offset (quantum well character of the s-Si channel) between the two devices. The plateau in the CV curve of the BC FET is a result of the accumulation of holes in the SiGe top layer under negative bias as described in [19]. Based on the results and discussing in [19], we conclude that the absence of a second plateau in the accumulation region and a plateau at higher voltages in the inversion region, proves that no parallel conduction is taking place in the s-Si BC MOSFET. This is also confirmed by the transconductance curves at low temperatures (10K<T<300K, not shown here) which do not show the double peaking attributed to parallel conduction that becomes more apparent at lower temperatures [20].

The minimum subthreshold slope S, in mV/decade, is given by Eq. 2,

$$S_{\min} = 10^3 \cdot \left(\max_{V_{GS}} \left\{ \frac{d \log_{10}(I_{DS}/I_0)}{dV_{GS}} \right\} \right)^{-1} \qquad (2)$$

where I_0=1A is a normalizing parameter.
S_{min} is given in Figure 5 as a function of gate length for both the s-Si BC and the Si control 2, and for three values of V_{DS}: 0.1, 1 and 1.5V. S_{min} is high for both structures due to the thick oxides and the relatively high doping in the substrate.

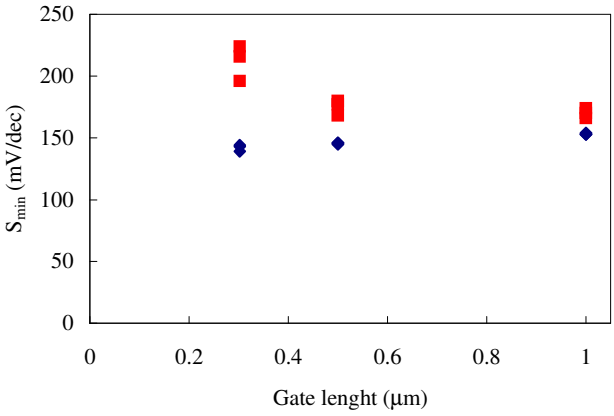

Figure 5: Minimum subthreshold slope as a function of gate length for three values of V_{DS}: 0.1, 1 and 1.5V. ■ s-Si BC FET. ♦ Si control 2. The bulk contact is connected to source (ground).

As expected, the sub-threshold slope of the Si control 2 is independent of the gate length and drain voltage due to the graded p-doping at the surface that controls the short channel effects (SCE). For the s-Si BC FET, deviation of the gate-length independent character of S happens at gate lengths L_g < 500nm. This is attributed to the weak control of the SCE in the BC device [21]. Also S_{min} is higher for the s-Si BC FETs with respect to their Si counterparts. MEDICI™ [22] simulations confirm that S remains slightly higher for the s-Si case compared to the Si control. MEDICI™ simulations predict a sub-threshold slope of S_{min}=115 mV/dec for s-Si BC and 100 mV/dec for Si control 2 at low drain bias. The experimental variation of S_{min} of the s-Si BC FET on the gate length and the drain bias is also confirmed by MEDICI™ simulations, showing a rapid increase for gate lengths L_g < 500nm and an increase as a function of increasing drain voltage.
Drain induced barrier lowering (DIBL) gives the influence of the drain voltage on the threshold voltage of the device. In this work, DIBL is determined from the shift of the log(I_{DS})-V_{GS} transfer curves at off-state between V_{DS}=0.1V (linear region) and V_{DS}=1V (saturation region). It should be noted that the value derived for DIBL is strongly dependent on the definition of the threshold voltage V_T. DIBL found using the minimum I_{DS} current to define V_T gives lower values than when V_T is determined by the tangent to the I_{DS}-V_{GS} curve at the point of maximum transconductance. This is confirmed by MEDICI™ simulations, in which the results are not influenced by

the imperfection in the material quality. DIBL derived via the second method for the different gate lengths is given in Figure 6. Again, short channel effects (SCE) are deteriorating the s-Si BC device faster than the Si control 2. The large values at short gate lengths are due to the HDD-only ohmic contact implant configuration presented here, the HDD-LDD configuration gives slightly lower values. For the s-Si BC FETs strategies for better control of the SCE have been proven difficult to implement [23]. Low power device technology though avoids aggressive scaling of the gate length because of the associated leakage current increase, therefore one can argue that the difficulty in scaling BC devices is not a major problems for low power applications.

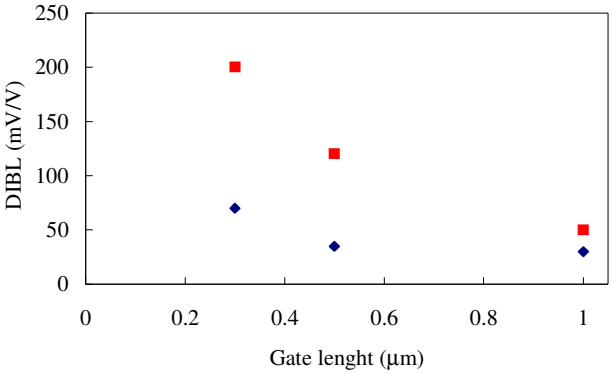

Figure 6: Drain induced barrier lowering (DIBL) as a function of gate length. DIBL is derived from the threshold voltage extracted via the maximum-transconductance-tangential approach. ■ s-Si BC, ♦ Si control 2.

Back-gating, where the bulk potential is different from the source potential, is studied in order to investigate the leakage currents expected in dynamic-threshold (DT) mode operation, a device configuration promising for low power applications [24]. It also gives information on the quality of the virtual substrate. The magnitude of the leakage current through the reverse biased drain/source-bulk pn-junction at room temperature is determined by the generation of minority carriers at defects in the material [7,24]. The off-leakage current remains low in the Si control (I_{off}=5.27 10^{-11} A at V_{BS}=0V and I_{off}=5.81 10^{-11} A at V_{BS}=-1V), but increases due to the dislocations in the virtual substrate in the s-Si BC device (I_{off}=7.61 10^{-11} A at V_{BS}=0V and I_{off}=8.61 10^{-10} A at V_{BS}=-1V). Although I_{on}/I_{off} at V_{BS}=0 is the same for both devices, the ratio lowers for the BC FET as a result of back-gating, given in Figure 7.

This result illustrates an important weakness of the virtual substrate approach – off-currents in the s-Si BC MOSFET can be strongly influenced by the material quality of the virtual substrate. Any ohmic contact implant touching the virtual substrate creates a potential route for leakage currents via the substrate. Therefore for good s-Si BC MOSFET the quality of the virtual substrate or good control over fabrication technology is essential [26].

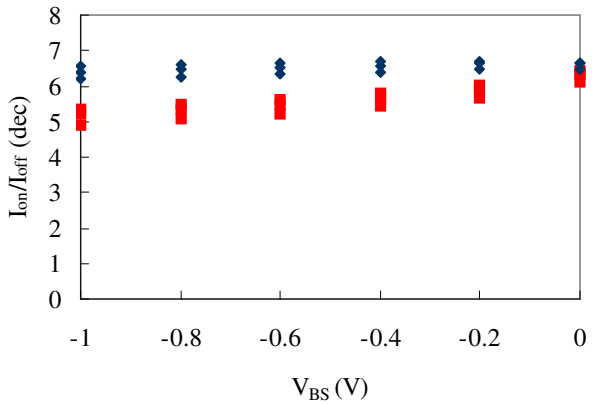

Figure 7: The ratio of the on and off current as a function of source-bulk voltage V_{BS} at V_{DS}=0.1V and for the 3 different gate lengths (decreasing gate length from top to bottom). ■ s-Si BC FET, ♦ Si control 2.

IV. High frequency characteristics

RF characteristics are measured using a 50GHz Agilent 8510C network analyser used over half its frequency range and controlled by Agilent ICCAP software. Three-step de-embedment was done using open, through and input- and output-side short in ICCAP. The de-embedded value of the cut-off frequency as a function of gate overdrive, V_{GS}-V_T for the 300 nm devices, is given in Figure 8 for the s-Si BC and the Si control 2.

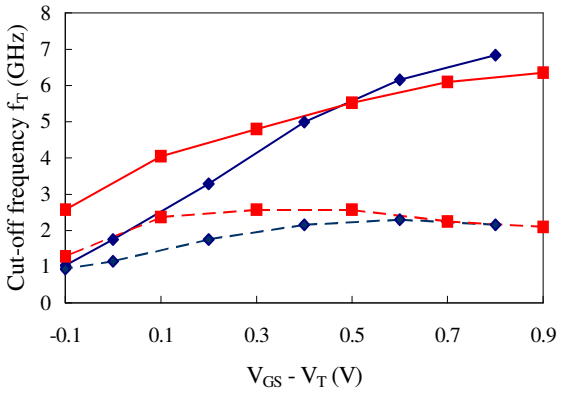

Figure 8: The de-embedded cut-off frequency as a function of gate overdrive for the s-Si BC MOSFET (■) and the Si control 2 (♦). The gate length is 300 nm. The full curves are for saturation operation at 1.2V V_{DS}, the dashed curves for triode region operation at 0.2 V_{DS}.

Although the values for the cut-off frequency are relatively small, the s-Si BC MOSFET out-performs the Si control 2 for small gate overdrive in both the triode and saturation region. The RF performance increase of the s-Si BC FET is especially large in the sub-threshold region, used for low power applications. The relatively low f_T values are attributed to the processing because no silicidation was used.

In order to study the influence of using a rather thick gate oxide of 20nm, the effect of the oxide thickness, t_{ox} on the cut-off frequency, f_T is studied analytically. Using the work of Y. Tsividis [26] we find the simplified expression for the cut-off pulsation ω_T of a MOSFET (when no velocity saturation occurs):

$$\omega_T = \frac{\mu(V_{GS} - V_T)}{\alpha L^2} \quad (3)$$

with μ the mobility, L the gate length and α the parameter used as an approximation to the slope of $-Q_b/C_{ox}$ with Q_b the depletion region charge per unit area and C_{ox} the oxide capacitance per unit area.

For low V_{DS}, a good approximation for α is given by [27]:

$$\alpha = 1 + \frac{dV_T}{dV_{SB}} = 1 + \frac{\gamma}{2\sqrt{\phi_0 + V_{SB}}} \quad (4)$$

with parameters as defined by (5).

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi_0 - V_{BS}} - \sqrt{\phi_0}\right), \quad (5)$$

where V_{T0} is the threshold voltage with V_{BS} = 0 V, and ϕ_0 is the value of the surface potential at the Si-SiO_2 interface at the onset of strong inversion [26]. α is closely related to the back-gating issue discussed in section III. The body effect parameters γ is inversely proportional to C_{ox} and thus proportional to t_{ox}. This makes the cut-off pulsation as given in (3) inversely proportional to t_{ox}. The back-gating measurements in section III allow us to derive the parameters γ and ϕ_0 for each device.

Using these values we find that α for the s-Si BC device at 1.14 is slightly larger than that for the Si control 2 at 1.13.

Using the measurements of $f_{T_{20nm}}$ for the t_{ox}=20nm devices, $\frac{\mu(V_{GS} - V_T)}{L^2}$ in (3) can be determined, and using γ_{3nm} = 3/20 γ_{20nm} in (4) together with V_{SB}=0, allows to estimate the cut-off frequency $f_{T_{3nm}}$ of the same devices if a 3nm gate oxide would have been used. The results are given in Figure 9 and predict that the s-Si BC MOSFET would out-perform the standard processed Si control 1 at low gate voltage overdrive. The maximum f_T for the Si control 1 is around 10GHz for a 300nm device (the low f_T value is a result of using a non-silicided ohmic contacts for Si control 1). An f_T value 2 times higher is expected for the s-Si BC MOSFET for this gate length.

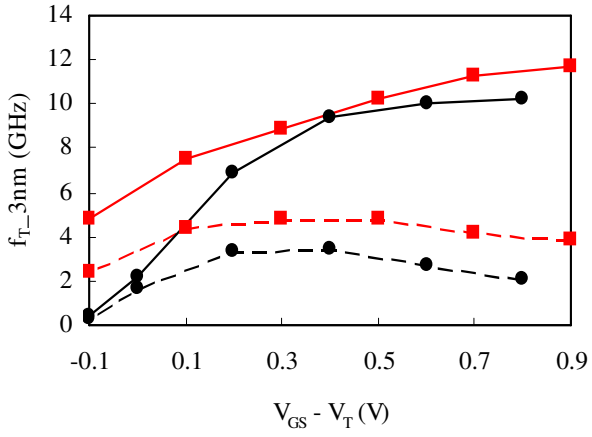

Figure 9: The de-embedded cut-off frequency as a function of gate overdrive for the predicted values of a 3 nm oxide s-Si BC MOSFET (■) using Eq. (4,5) and the Si control 1 (♦). The gate length is 300 nm. The full curves are for saturation operation at 1.2V V_{DS}, the dashed curves for triode region operation at 0.2 V_{DS}.

V. Conclusions

The influence of the retention of the material integrity during low temperature processing out-weights the increased contact resistance in the s-Si BC MOS-gated FETs, especially in the region of low gate voltage overdrive. The use of ultra-thin modulation doped layers, together with a selective TMAH etch has been proven to remove the parallel conduction in the BC devices.

RF measurements show that the s-Si BC MOS-gated FET outperforms the Si control which underwent the same processing. It is predicted, using parameters extracted from back-gating measurements, that the performance of the s-Si BC MOSFET with a reduced gate oxide thickness (3nm) would outperform the full thermal budget Si MOSFET.

The I_{on}/I_{off} of both devices is similar at a value of 6. I_{off} in the s-Si BC MOSFET however increases rapidly with back-gating, related to the dislocations in the virtual substrate. The minimum sub-threshold slope and DIBL were found to be more sensitive to downscaling in the s-Si BC MOSFET.

These measurements has shown that MOS-gated strained-Si buried channel FETs have excellent potential for low power applications.

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