# Single Device Logic using 3D Gating of Screen Grid Field Effect Transistors

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***Abstract*—The Screen Grid Field Effect Transistor (SGrFET) is an oxide-gated FET with a novel 3D gating configuration perpendicular to the current flow in the channel. The multiple gate character of the SGrFET lends itself perfectly to compact logic applications with a reduced number of devices per gate. In this report TCAD results of both DC and transient performance of double-gate row SGrFET logic are presented. The analysis of both the complementary and the all-n-type SGrFET inverter logic gives ps rise times and large noise margins up to 400mV for 1V supply. NAND, NOR and XOR logics can be obtained using only two n-type SGrFETs.**

***Index Terms*—**FETs, semiconductor device logic, transient analysis, semiconductor device modeling.

## I. Introduction

As CMOS is scaling down with the aim of increasing operation speed and decreasing device area, the need for better control of the channel by the gate has driven research towards devices with multiple gate configurations. Different types of multiple gate FETs have been proposed of which the finFET with a 2, 3 or even 4 gate configuration is the most popular. Amongst the FETs with other multiple gate configurations is the Screen-Grid Field Effect Transistor (SGrFET) [1]. As the finFET, the SGrFET is defined on SOI (Silicon-On-Insulator), but its gating approach is completely different as can be seen in Fig. 1. No fins are needed as the SGrFET is planar. The gate consists of oxide cylinders (fingers) with a poly-Si or metal core. These fingers are placed perpendicular to the current flow in the channel. Different gate configurations are possible, as explained in [1] but the most straightforward one that also gives excellent control on sub-threshold slope and drain induced barrier lowering (DIBL) is the two gate row configuration shown in Fig. 1. Increasing the current drive can be obtained by widening the device (and accordingly expanding the gate's grille), but unlike in conventional SOI technology the increase can also be obtained by increasing the body height without any detrimental effect to the gate control (DIBL, Short-Channel Effect (SCE), …). Highly doped source and drain areas are located at both sides of the device and have the same width as the device, avoiding contacting problems to small areas. For optimum performance the channel doping is low to un-doped in order to preserve high mobility values and of the same doping type as the contact regions unlike traditional MOSFETs. The device operation is essentially based on the control of the carrier concentration between the gate fingers in the first row (the one closer to the source contact). The main role of the second row of fingers (the one close to the drain contact) is to screen the electrical action of the drain on the above mentioned carrier concentration, therefore the second row controls the amount of DIBL and SCE in downscaled SGrFETs. The SGrFET performs best in sub-threshold and weak inversion, in these regimes high mobility values can be expected due to reduced surface scattering because the carriers flow away from the cylinder's walls.

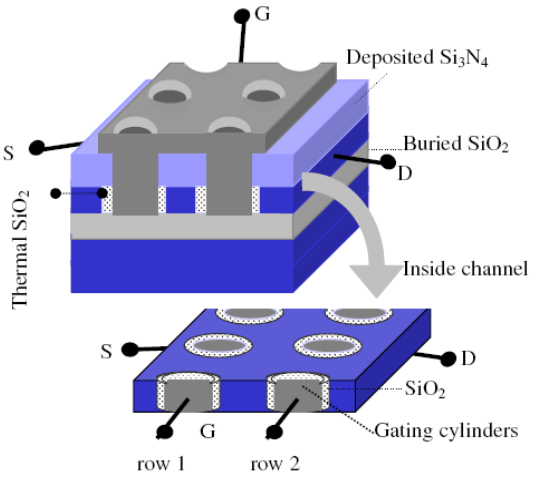


Figure 1: Schematic configuration of a SGrFET with two gating rows, each consisting of 3 gate cylinders.

The threshold voltage of the SGrFET can be controlled, as in finFETs, via an appropriate choice of the gate workfunction, Table 1 shows the threshold voltage ($V_{th}$) values for two different gate's metals.

| Device Type | $V_{th}$ (V) | Metal Work Function (V) | Example of Gate Contact |
|---|---|---|---|
| n-SGrFET | 0.44 | 4.8 | Gold |
| p-SGrFET | +0.3 | 4.8 | Gold |
| n-SGrFET | -0.2 | 4.10 | Aluminum |

Table 1: Device type as a function of work function

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## II. DC ANALYSIS

The split-gate configuration of the SGrFET, where gate row 1 and 2 are not interconnected, lends itself ideally for mixing and single device logic. This increased functionality of the SGrFET can be exploited for digital applications by applying synchronous or asynchronous voltages on the two gate finger rows.

For the simulations, in 2D, we have used Medici™ [3]. 2D simulations are done on the cross section plane from source to drain parallel to the semiconductor/buried oxide surface. The hydrodynamic (HD) model has been used for DC simulations as the length of the active region is under a quarter micron, nevertheless the DC results obtained from drift-diffusion (DD) and HD models were similar. According to this, the DD model was used for transient analysis in order to save CPU time and prevent the appearance of convergence problems. The gate oxide thickness is 2 nm, the source-drain distance 240 nm, the diameter of the gate cylinders 50 nm and the distance between the outer edges of the gate cylinders 40 nm. Where necessary the SOI body thickness is assumed to be 100 nm. For the DC evaluation of the split-gate performance an n-type SGrFET is used with un-doped channel area ($N_D = 10^{15}$ cm$^{-3}$) and highly doped drain and source regions ($N_D = 10^{19}$ cm$^{-3}$). In order to enhance the calculation speed one unit cell with four half gate circles is used similar to [1]. N unit cells will give N times the current drive of 1 unit cell. Fig. 2 shows the DC transfer characteristics for the split-gate functioning of the n-SGrFET. In these simulations the voltage of one gate row (with reference to Fig.1: gate row 1 = G-S, gate row 2 = G-D) is kept constant at a high (H=1V) or low (L=-0.3V) voltage level whilst the voltage on other gate row changes gradually between these two value. The source-drain voltage is kept at $V_{DS}$=1V. The threshold voltage of the device when all gates swing between H to Lis $V_{th}$=0.44V.

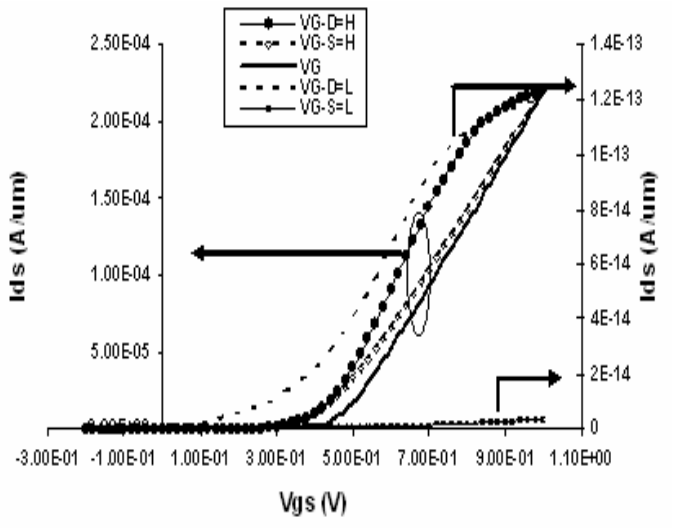


Figure2: Transfer characteristics of the DC sweep of one gate row with the other gate row voltage constant. $V_{DS}$=1 V. ( ——●—— ) $V_{G-D}$=H, $V_{G-S}$ swings ( ——▪—— ) $V_{G-D}$=L, $V_{G-S}$ swing ( —◆— ) $V_{G-S}$=H $V_{G-D}$ swings ( ——▸—— ) $V_{G-S}$=L, $V_{G-D}$ swings, ( ——— ) $V_G$ swings

The values for the high and low gate voltage are those for which the device is respectively ON and OFF, given by [2]:

$$V_{ON} = V_{DD} + V_{th} \qquad V_{OFF} = -V_{th} \qquad (1)$$

| Configuration | $V_{th}$ (V) | S(mV/dec) |
|---|---|---|
| $V_{G-D}$=H, $V_{G-S}$ swings | 0.4 | 68.40 |
| $V_{G-D}$=L, $V_{G-S}$ swing | 0.16 | 158.2 |
| $V_{G-S}$=H ,$V_{G-D}$ swings | 0.3 | 80.20 |
| $V_{G-S}$=L, $V_{G-D}$ swings | 0.17 | 186.9 |
| $V_G$ swings | 0.4 | 61 |

Table 2: DC Parameters of Split-Gate SGrFET operation.

When one of the gate rows is kept at OFF, the drain current is very low and the sub-threshold slope, S, is very high. This is a result of the efficiency of the pinch-off of the channel with one single gate row. Opening of a part of the channel region by increasing the voltage on the other gate row does not allow the SGrFET to switch on. However, when one of the gate rows is ON, currents increase and S decreases to near optimal values. The threshold voltage shifts between H and L state, creating the possibility for single device logic. Table 2 summarizes these results.

## III. ANALYSIS OF LOGIC CIRCUITS

In this section we first investigate the SGrFET in classical complementary and all-n-FET (Enhancement-Depletion, EDMOS) inverter circuits where the same voltage is applied to both gate rows. Then a two-device NAND, NOR and XOR are also investigated where the split-gate configuration discussed in section II is exploited to make the circuit more compact. Both DC and transient analysis will be presented.

### *A. Inverter circuits*

Two possible configurations are studied, the complementary C-SGrFET and the n-SGrFET EDMOS inverter. "ON" and "OFF" gate voltages are as defined in Eq. (1): $V_{ON}$ = 1.4V and $V_{OFF}$=-0.4V for the n-type and $V_{ON}$= -1.3V and $V_{OFF}$= 0.3V for the p-type SGrFET. The load in the n-SGrFET inverter is a depletion mode n-SGrFET with $V_{th}$= -0.2. Thus, when the driver is working in the linear region with unit receptivity, the

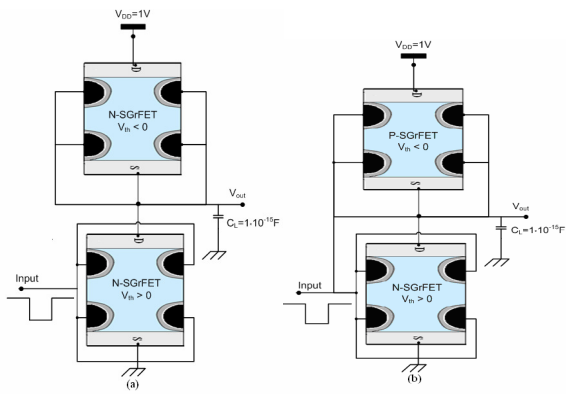


Figure 3: (a) n-SGrFET inverter, (b) C-SGrFET inverter.

load is in its saturation region. The supply voltage $V_{DD}$=1V in both cases.

Both inverter circuits are given in Fig. 3. The value of the capacitive load, $C_L$ in Fig. 3 is chosen as the input capacitance of the following SGrFET (its value can be changed to accommodate the fan-out of a specific circuit). To estimate $C_L$ we compose the oxide capacitances of the 4 half gate cylinders (this result is close to that extracted from AC simulations):

$$C_L = 2\varepsilon_{ox}\varepsilon_o \frac{(2\pi r_{in})}{t_{ox}} h \qquad (2)$$

Where $\varepsilon_{ox}$ is the permittivity of the oxide; $\varepsilon_0$ is the permittivity of vacuum; $h$ is the thickness of the Si channel; $t_{ox}$ is the gate oxide thickness and $r_{in}$ is the inner radius of the gate cylinder.

Fig. 4 shows the DC transfer characteristics of both inverter circuits.

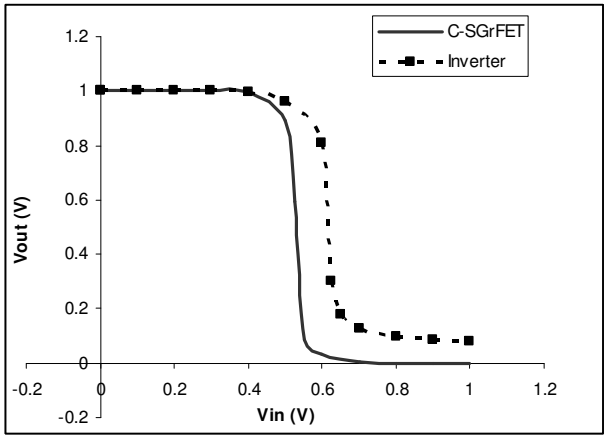


Figure 4: Comparison of the transfer characteristics of the n-SGrFET (dashed line) and C-SGrFET (full line) inverter.

The C-SGrFET provides better performance than the n-SGrFET inverter, similar to other CMOS technologies. Power consumed in the C-SGrFET circuit is also lower because current is only drawn when switching [3] whilst for the n-SGrFET inverter a small current is flowing for high input voltages on the gate.

The rise time ($t_r$) is defined as the time taken for the output voltage to go from 10% to 90% of its final value, $t_r$=4 ps.

The noise margins (NM) of both types of inverters are extracted following the standard procedure [5]. There are two different noise margins, one for H (1V) and one for L (-0.3V). These NMs are given by [4] (we use the same notation as in ref. [4]): $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$. The results are summarized in Table 3.

| Inverter | $V_{OL}$ (V) | $V_{OH}$ (V) | $V_{IL}$ (V) | $V_{IH}$ (V) | $NM_L$ (V) | $NM_H$ (V) |
|---|---|---|---|---|---|---|
| Fig.3a | 0.15 | 0.92 | 0.55 | 0.67 | 0.4 | 0.25 |
| Fig.3b | 0.06 | 0.95 | 0.47 | 0.57 | 0.31 | 0.38 |

Table 3: Noise Margin and On-OFF region for both n- and C-SGrFET inverter (resp. Fig.3a & Fig.3b)

### B. NAND Logic

One of the key features in SGrFETs is its multi-gate functionality. A two-device NAND (Fig. 5 (a)) can be generated using the split-gate character presented in section II. Figure 5 (b) shows the transient analysis of the NAND logic.

Although the OFF state is not zero for the chosen SGrFETs, this problem can be alleviated by increasing the size of the driver to compensate for the discharge pull-down [6].

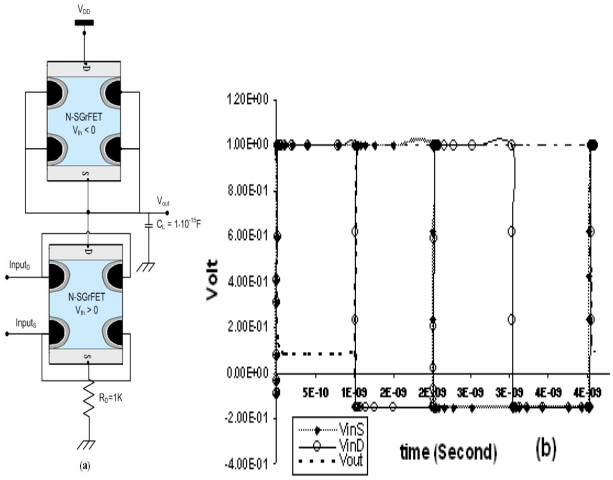


Figure 5: (a) Schematic circuit of a SGrFET NAND (b) NAND Output/Inputs Voltages vs. time

### C. NOR Logic

NOR logic is presented using two devices, a n-SGrFET as follower and a p-SGrFET as driver. Fig. 6 shows the schematic circuit and transient response. The NOR operation is achieved with $W_{P\text{-}SGrFET} / W_{N\text{-}SGrFET} = 4$ where the effective width of SGrFET is defined as the outer distance between two gate cylinders in one row.

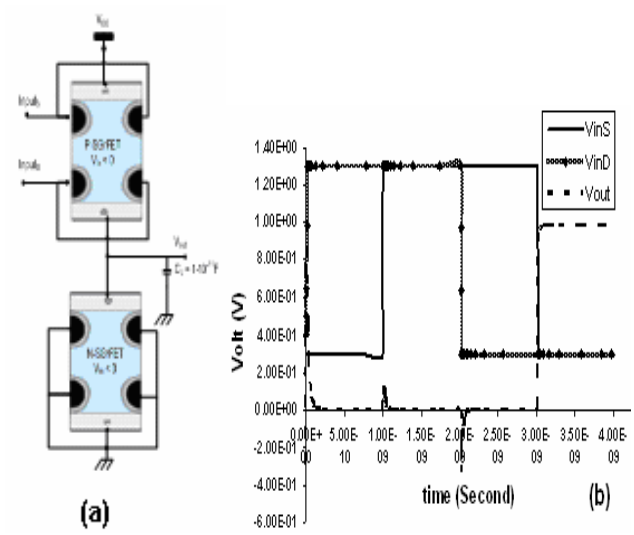


Figure 6: (a) Schematic circuit of a SGrFET NOR (b) NOR Output/Inputs Voltages vs. time

### D. XOR Logic

An XOR circuit can be constructed with only two SGrFETs. We present two different ways to implement the SGrFET XOR circuits. The difference is based on the number of gate cylinders in the driver. As demonstrated in [1] the width of the SGrFET can be increased by adding additional unit cells. This increases current drive whilst retaining the other FET parameters. This feature will be exploited in the XOR driver. Figure 7 and 8 give respectively an XOR with a single and triple unit cell driver.

The XOR with one unit cell uses the width relationship:
$W_{N\text{-}SGrFET} / W_{P\text{-}SGrFET} = 7$.

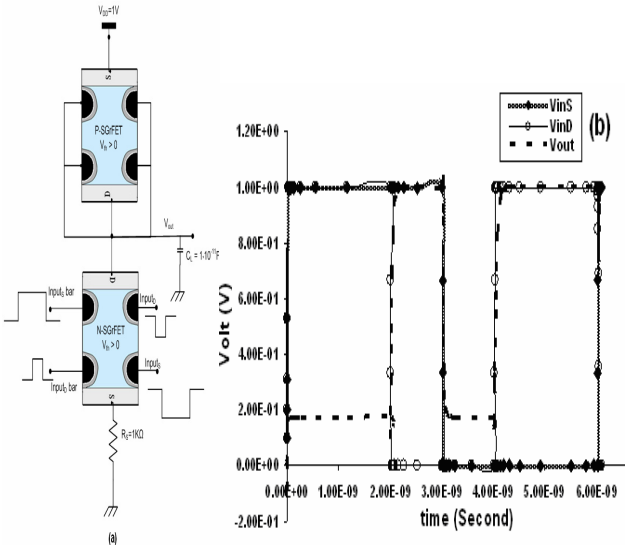


Figure 7: (a) Schematic circuit of a SGrFET XOR (b) XOR Output/Inputs Voltages vs. time

From Fig. 7b it is clear that when both inputs are low or high, $V_{out}$ is not completely OFF. This is similar to the NAND (Fig.5). This problem can be solved by using a SGrFET with three unit cells as a driver as shown in Fig. 8. The output of the XOR with the 3-unit-cell driver switches completely off as can be seen from Fig. 8b. This approach can also be applied in the previously presented logic circuit to ensure the OFF state consumed minimum current.

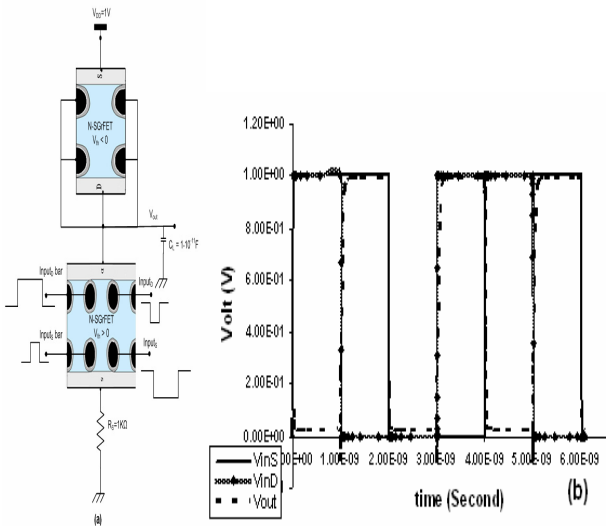


Figure 8: (a) Schematic circuit of a SGrFET XOR with triple unit cell driver (b) XOR Output/Inputs Voltages vs. time

Note that the effective channel width in the SGrFET with 3 unit cells is *3xW* with *W* the distance between the gate cylinders in one row (width of one unit cell).

## IV. CONCLUSION

In this report we presented the simulated DC and transient performance of the SGrFET with independent double gate for digital applications. First the SGrFET was used in a classical circuit configuration with connected gate fingers and the transient performance of C-SGrFET and EDMOS inverter was presented. The results demonstrate the superior performance of the complementary approach with ps switching times and 0.4V maximum noise margin.

In the second part of the paper the multi-functionality offered by the SGrFET in the independent double gate configuration was exploited in three logic circuits: NAND, NOR and XOR, which can all be realized using only two SGrFETs. Switching times are of the order of ps. It was demonstrated that the OFF state in the logic circuits can be improved by using a SGrFET driver with an appropriate number of unit cells. For the SGrFET a multi-unit cell approach is not more complicated from a device fabrication point of view than a single unit cell approach.

These simulation results demonstrate the potential advantage of using a SGrFET for logic applications.

## ACKNOWLEDGMENT

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